TABLE OF CONTENTS

SECTION		PAGE	
I	INTRODUCTION	1	1/A12
	A. Frequency Domain Correlation	3	1/B1
	B. Time Domain Correlation	8	1/B6
II	32-POINT CCD CZT IC	14	1/B14
	A. Chip Overview	14	1/B14
	B. CCD Filter	22	1/C13
	C. Operational Amplifiers	27	1/D6
	1. Design	27	1/D6
	2. Experimental Results	52	1/F12
	D. Multiplying Digital-to-Analog Converters (MDACs)	59	1/G11
	1. Design	59	1/G11
	2. Experimental Results	71	2/A14
	E. Read-Only Memory (ROM) and ROM Address	71	2/A14
	1. Read-Only Memory	71	2/A14
	2. Up/Down Ring Counter (ROM Address)	82	2/C3
	3. Synchronization	87	2/C9
	F. Timing Circuitry	98	2/D10
	1. Clock Generators	98	2/D10
	2. Experimental Results	109	2/E10
	G. Experimental Results	114	2/F3
	H. Applications	121	2/F11
III	64-POINT CCD ANALOG/ANALOG CORRELATOR	125	2/G5
	A. Design	125	2/G5
	B. Performance Limitations in Design	129	2/G12
	1. Multiplier Nonlinearity	129	2/G12
	2. Offsets	132	3/A4
	3. Input Stage Offsets and Nonlinearities	133	3/A5
	C. Measured Performance	133	3/A5
	1. CCD Signal Capacity	133	3/A5
	2. Feedback Linearized Input Stage	134	3/A6

TABLE OF CONTENTS

(Continued)

SECTION PAGE

3. Multiplier Linearity. 136 3/A8
4. Offsets 140 3/A13
5. Multiplier Scale Factor Matching. 148 3/B7
6. Evaluation. 148 3/B7
D. Directions for Future Designs. 150 3/B9
1. System Organization 150 3/B9
2. CCD Design. 152 3/B11
3. Input Stage Design. 152 3/B11
4. Buffer Design 152 3/B11
5. Multipliers 153 3/B12
E. Applications and Summary 153 3/B12
1. Applications. 153 3/B12
2. Summary 153 3/B12
IV CCD BINARY/ANALOG CORRELATOR. 155 3/B14
A. Introduction 155 3/B14
B. Binary/Analog Programmable CCD Correlator Technology 159 3/C4
C. Application of Binary/Analog Correlator to Pattern Classification 171 3/D7
D. Preliminary Design of Matrix Multiplier IC 174 3/D10
E. Four-Sensor Demonstration Unit 177 3/D13
V CONCLUSIONS 182 3/E4
REFERENCES. 184 3/E6

LIST OF ILLUSTRATIONS

FIGURE PAGE

1 Block Diagram of a Transversal Filter Showing Delay Stages D and Weighting Coefficients h_n n = 0, N - 1. 2
2 Schematic of the CZT Algorithm. 5
3 Interpretation of the CZT in Terms of Chirp Input Waveforms in Chirp Filters. 6
4 Block Diagram of a CCD Programmable Correlator. 7
5 Block Diagram of the Analog/Analog Time Domain Correlator 9
6 Circuit Schematic of the Four-Quadrant Multiplier Used in the Analog/Analog Correlator of Figure 5. 10

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Low Power, Compact Charge Coupled Device Signal Processing System

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C. R. Hewes, and D. J. Mayer

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Texas Instruments Incorporated
Dallas, Texas

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**Scientific and Technical
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1980

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TABLE OF CONTENTS

(Continued)

SECTION PAGE

3. Multiplier Linearity. 136
4. Offsets 140
5. Multiplier Scale Factor Matching. 148
6. Evaluation. 148

D. Directions for Future Designs. 150
1. System Organization 150
2. CCD Design. 152
3. Input Stage Design. 152
4. Buffer Design 152
5. Multipliers 153

E. Applications and Summary 153
1. Applications. 153
2. Summary 153

IV CCD BINARY/ANALOG CORRELATOR. 155
A. Introduction 155
B. Binary/Analog Programmable CCD Correlator Technology 159
C. Application of Binary/Analog Correlator to Pattern Classification 171
D. Preliminary Design of Matrix Multiplier IC 174
E. Four-Sensor Demonstration Unit 177

V CONCLUSIONS 182

REFERENCES. 184

LIST OF ILLUSTRATIONS

FIGURE PAGE

1 Block Diagram of a Transversal Filter Showing Delay Stages D and Weighting Coefficients h_n n = 0, N - 1. 2
2 Schematic of the CZT Algorithm. 5
3 Interpretation of the CZT in Terms of Chirp Input Waveforms in Chirp Filters. 6
4 Block Diagram of a CCD Programmable Correlator. 7
5 Block Diagram of the Analog/Analog Time Domain Correlator 9
6 Circuit Schematic of the Four-Quadrant Multiplier Used in the Analog/Analog Correlator of Figure 5. 10

LIST OF ILLUSTRATIONS

(Continued)

FIGURE PAGE

7 Block Diagram of the Binary/Analog Correlator 12

8 Block Diagram of 32-Point CZT IC. 15

9 Photomicrograph of 32-Point CCD CZT IC. 16

10 Silicon Gate CCD Coplanar Electrode Structure 17

11 Block Diagram of Internal ROM, Up/Down Counter, and Dual MDACs. 19

12 Block Diagram of Second Dual MDAC 20

13 Block Diagram of CCD Input Amplifiers, CCDs, DCI, and Output Buffers. 21

14 Photomicrograph of CCD Transversal Filters. 23

15 Schematic of CCD Filters. 24

16 CCD Timing. 26

17 CCD Capacitances. 28

18 A Possible Switching Diagram for Figure 17. 29

19 Symmetrized and Compensated Two-Phase CCD Layout. 32

20 DCI Amplifier Compensated for Gain of 30. 34

21 Photomicrograph of Operation Amplifier Used on CZT IC . . . 35

22 Block Diagram of Single-Loop Amplifier. 40

23 Differential Amplifier. 41

24 Differential Amplifier Theoretical Open Loop Characteristics 43

25 Input Amplifier Closed Loop Frequency Response. 44

26 DCI Amplifier 45

27 DCI Timing. 46

28 CCD Clocks. 48

29 Model for DCI 50

30 Capacitance Model for DCI Input 51

31 DCI Diff-Amp Open Loop Performance. 53

32 Closed Loop Frequency Response of DCI Amplifier 54

33 Differential Amplifiers Test. 55

34 Single-Ended Transfer Characteristics of Input Differential Amplifier. 56

LIST OF ILLUSTRATIONS

(Continued)

FIGURE PAGE

35 Response of Input Differential Amplifier to Common Mode Input. 57

36 Differential Mode Characteristics of Input Amplifier. . . . 58

37 Single-Ended Response of Differential Amplifier to Ramp Input 60

38 Photograph Showing the Gain and Linearity of Input Amplifiers. 61

39 DCI Amplifier Open Loop Characteristics 62

40 Photograph of Dual MDACs Used on CZT IC 63

41 MDAC 64

42 Buffered Input Sample-and-Hold. 67

43 ROM Sense and MDAC Drive Circuitry. 69

44 Typical MDAC Operation (Multiplication by 0.5). 70

45 Transfer Curve for Input Sample-and-Hold Circuit of MDAC. . 72

46 Block Diagram of MDAC Test. 73

47 Response of MDAC to dc Input and Sine Chirp of Internal ROM $(V^+ - V^-) < 0$ 74

48 Relative Accuracy of MDACs. 76

49 8-Bit by 17-Word ROM (Sine Chirp Coded) 78

50 Photograph of ROM 80

51 Analog Representation of Sine Chirp Coded into ROM. 81

52 Three-Stage Up/Down Ring Counter. 83

53 Typical Shift Register Operation (SRO). 84

54 Up/Down Counter Waveforms - Normal Operation. 88

55 Photograph of Up/Down Counter 89

56 Synchronization of Two CCD CZT ICs. 91

57 External Sync Pulse Generator 92

58 External Sync Pulse Generator Timing - Normal Operation . . 93

59 GEN 30 (Internal Sync Pulse). 95

60 GEN 30 Timing 96

61 Synchronization Outputs of Two CZT ICs Operating Together . 97

62 Block Diagram of Clock Generators 99

LIST OF ILLUSTRATIONS

(Continued)

FIGURE		PAGE
63	G1 Clock Pulse Generator	100
64	CCD $\phi_2^{\pm}$ Clock Pulse Generator	102
65	G3 Inverter	103
66	G4 Inverter	104
67	G5 Generator	105
68	G6 Generator	106
69	Connections of the Clock Generators Showing Capacitive Load of Each Driver	107
70	System Timing	110
71	Clock Circuit Performance	111
72	Relationship of ϕ_B and ϕ_C	112
73	Photograph of CCD ϕ_2 Clock Driver	113
74	A System for Obtaining Power Density Spectrum of a Real Input Using One CZT IC (50% Input/Output Duty Cycle)	115
75	Operation of CCD CZT IC with 10 kHz Clocks	116
76	Operation of CCD CZT IC with 1 MHz Clocks	117
77	Power Density Spectra for Three Sine Waves Obtained Using the 32-Point CCD CZT at a 10 kHz Sample Rate	118
78	Power Density Spectra for Three Sine Waves Obtained Using the 32-Point CCD CZT at 1 MHz Sample Rate	119
79	Response of CCD CZT IC to Square-Wave Inputs (10 kHz Clock Frequency)	120
80	Realization of Complex I/O CZT with One Chip (50% Duty Cycle)	122
81	Realization of Complex I/O CZT Using Two CZT ICs (100% Duty Cycle)	123
82	Realization of Correlator Using Two CZT ICs (Real 25% Duty Cycle Input, Real 50% Duty Cycle Output)	124
83	Analog Correlator Block Diagram	126
84	Floating Gate Reset Technique	127
85	Analog Multiplier	128
86	CCD Input Stage	130
87(a)	CCD Input Stage Feedback-Linearized Output	135
87(b)	CCD Serial Output vs Input	135

LIST OF ILLUSTRATIONS

(Continued)

FIGURE		PAGE
88(a)	CCD1 Serial Output Linearity 0.4 V_{pp} Signal	137
88(b)	CCD1 Serial Output Linearity 0.5 V_{pp} Signal	137
89(a)	CCD2 Serial Output Linearity 0.4 V_{pp} Signal	138
89(b)	CCD2 Serial Output Linearity 0.55 V_{pp} Signal	138
90	Multiplier Linearity Test Circuit	139
91(a)	Multiplier Output $V_{in} = \pm 0.3\ V_{pk}$	141
91(b)	Multiplier Output $V_{in} = \pm 1\ V_{pk}$.	141
92(a)	Convolution of Two 300 mV Impulses (CCD2 Offsets).	142
92(b)	Convolution of Impulse with CCD Offsets (CCD1 Offsets).	142
93(a)	CCD1 Frequency Domain Offset Measurements (Low Pass Output to 2.5 kHz).	145
93(b)	CCD1 Low Pass and Offset Error Outputs to 10 kHz (Offset Error Output)	145
94(a)	CCD1 Low Pass and Offset Error Outputs to 2.5 kHz	146
94(b)	CCD2 Low Pass and Offset Error Outputs to 2.5 kHz	146
95(a)	CCD2 Low Pass Output to 25 kHz.	147
95(b)	CCD2 Offset Error Output to 25 kHz	147
96(a)	Multiplier Scale Factor Accuracy; Convolution of CCD1 (Impulse of Four Samples) with CCD2 (Full Scale Dc) . . .	149
96(b)	Multiplier Scale Factor Accuracy; Multiplier Scale Factor Error.	149
97(a)	64-Point Convolution of Two Low-Frequency Triangle Waves	151
97(b)	64-Point Convolution of Two Low-Frequency Square Waves	151
98	Block Diagram of the Binary/Analog Correlator	160
99	Schematic of the Operation of the Programmable CCD Correlator.	162
100	Schematic of a Programmable CCD Correlator with M-Bit Accuracy on the Weighting Coefficients.	165
101	Shift Register and Clock Generator for CCD Correlator . .	166

LIST OF ILLUSTRATIONS

(Continued)

FIGURE		PAGE
102	Photograph of a 32-Stage Binary/Analog Correlator with Four-Bit Weighting Coefficients	167
103	Experimental Impulse Response of 32-Stage Binary/Analog Convolver	168
104	Response of the Test Device Operated as a Bandpass Filter	169
105	Frequency Response of the Binary/Analog Correlator Programmed to Give a Bandpass Filter with Passband at 125 kHz	170
106	Matched Filter Operation of the Test Device Using a 13-Bit Barker Code	172
107	Block Diagram for Computing $Y^T Y$	173
108	Block Diagram of Binary/Analog Correlator IC	175
109	Preliminary Design of Four-Column by 16-Stage by Eight-Bit CCD Matrix Multiplier IC	176
110	System Block Diagram for Pattern Classifier	178
111	Block Diagram of Pattern Classifier Using 32 x 2-Bit Binary/Analog Correlator	179
112	Illustration of 8-Bit Accuracy of the Binary/Analog Correlator	181

LIST OF TABLES

TABLE		PAGE
I	FET Geometries and Supplies	36
II	MDAC Error	75
III	MDAC Characteristics	77

SECTION I

INTRODUCTION

The mathematical operation of convolution is a very important function in many of the pattern recognition or pattern classification algorithms that are used to synthesize useful information about the earth from the electrical outputs of satellite-borne environmental sensors. Since charge coupled devices (CCDs) are so well suited to performing convolution, it is not surprising that substantial interest has arisen within NASA in developing CCDs for preprocessing environmental sensor data preparatory to its transmittal to the ground.

The one complication that limits the immediate usefulness of CCDs is the fact that the satellite preprocessors are learning machines[1] and must adapt to the terrain they are observing. In terms of CCD hardware, this means that the convolutions must be programmable; i.e., the impulse responses of the filters must be electronically variable.

The canonical CCD transversal filter, illustrated in Figure 1, has fixed weighting coefficients h_n $n = 0, N - 1$ that are coded into the photomask with which the device is made. The impulse response is determined by the h_n and is not electrically alterable. Various approaches have been tried to construct filters with electronically alterable h_n,[2,3] but all such attempts have failed to maintain the electronic simplicity of the fixed weighting coefficient transversal filter.

This program addresses two different techniques for performing programmable correlation

- Frequency domain correlation using the CCD chirp z-transform (CZT).
- Time domain correlation using direct analog/analog correlation and binary/analog correlation.

Two separate ICs have been developed under the program:

- 32-point CCD CZT IC.

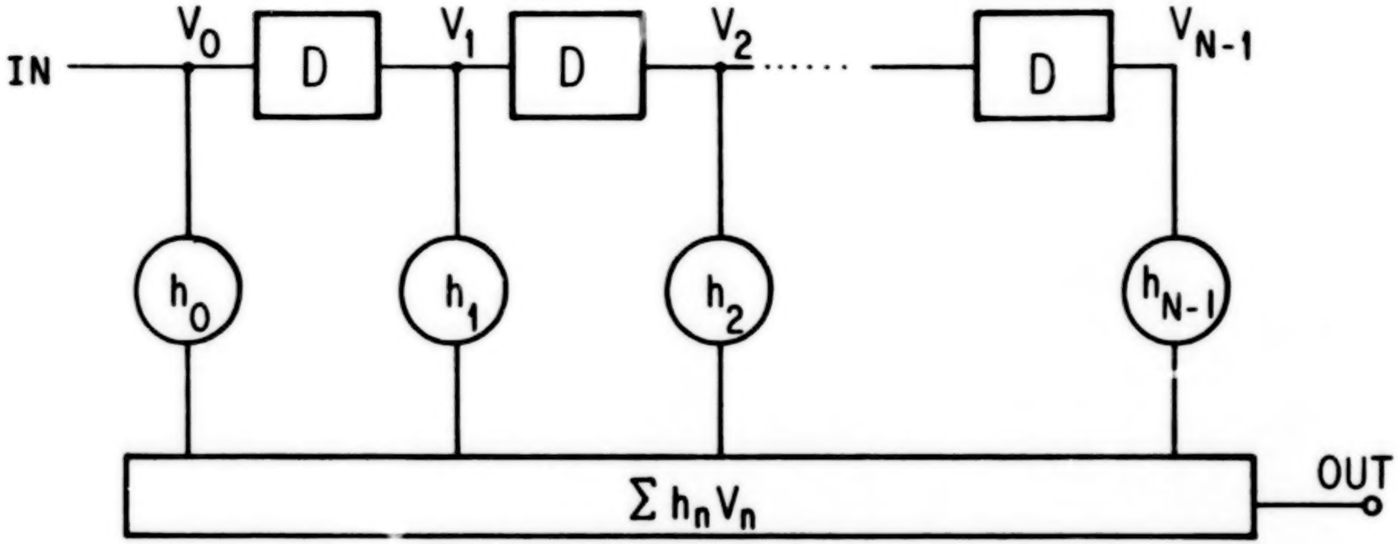

IN
V_0
D
V_1
D
V_2
D
V_{N-1}
h_0
h_1
h_2
h_{N-1}
$\sum h_n V_n$
OUT

Figure 1.- Block Diagram of a Transversal Filter Showing Delay Stages D and Weighting Coefficients h_n n=0, N-1.

- 32-point CCD analog/analog correlator.

These two ICs are discussed in Sections II and III, respectively. In addition, a prototype IC capable of correlating a digital reference word with an analog input signal was evaluated under this program. The evaluation of the binary/analog correlator is discussed in Section IV.

A. Frequency Domain Correlation

This approach to programmable correlation is based on the fact that correlation in the time domain is equivalent to multiplication in the frequency domain. Consequently, the frequency domain correlator is based on taking the discrete Fourier transform (DFT) of the input signal.

The discrete Fourier transform operation can be performed using the chirp z-transform algorithm.[4] The CZT gets its name from the fact that it can be implemented in an analog manner by (1) premultiplying the time signal with a chirp (linear FM) waveform, (2) filtering in a chirp convolution filter, and (3) postmultiplying with a chirp waveform.

When implemented digitally, the CZT has no advantages over the conventional fast Fourier transform algorithm.[4] However, the algorithm lends itself naturally to implementation with CTD transfersal filters.[5,6]

Starting with the definition of the DFT

$$F_k = \sum_{n=0}^{N-1} f_n e^{-i2\pi nk/N} \tag{1}$$

and using the substitution

$$2nk = n^2 + k^2 - (n - k)^2 \quad , \tag{2}$$

the following equation results.

$$F_k = e^{-i\pi k^2/N} \left[\sum_{n=0}^{N-1} \left(f_n e^{-i\pi n^2/N} \right) e^{i\pi (k-n)^2/N} \right] \quad . \tag{3}$$

This equation has been factored to emphasize the three operations that make up the CZT algorithm. It is illustrated in Figure 2.

To implement the conventional N-point CZT, the CCD filters are chirp filters of length 2N-1 that chirp from $-f_c$ to $+f_c$, and the premultiply waveform has a time duration N/f_c and chirps from zero to $-f_c$. A physical interpretation in terms of correlation of the input chirp with the filter is given in Figure 3. When the input signal has zero frequency, the product with the premultiply chirp results in an input waveform to the filter that chirps from 0 to $-f_c$. The samples corresponding to frequencies near $f = 0$ are clocked into the filter first, and those near $f = -f_c$ are clocked in last. This sequence of samples results in a correlation peak at $t = t_o$, when the product waveform has been clocked into the first half of the filter. When the input frequency is $f_1 \neq 0$, the product with the premultiply chirp results in an input to the filter that chirps from f_1 to $-f_c + f_1$. The input waveform (V_{in} x chirp) in Figure 3 corresponds to an input signal at a frequency f_1 at time $t = t_o$. This waveform is shifted to the right as t increases, resulting in a correlation peak at t_1. The shift in time relative to the dc correlation peak is

$$t_1 - t_1 = \frac{N}{f_c^2} f_1 \quad . \tag{4}$$

In this way, the time axis of the output is calibrated in frequency.

The CZT is very convenient for performing programmable correlation. Figure 4(a) shows that correlation of x(t) with h(t) can be accomplished by (1) performing the discrete Fourier transform (DFT) of x(t) to obtain X(f); (2) multiplying X(f) by H(f), where H(f) is the DFT of h(t); and (3) performing the inverse DFT on Y(f) = X(f) · H(f).

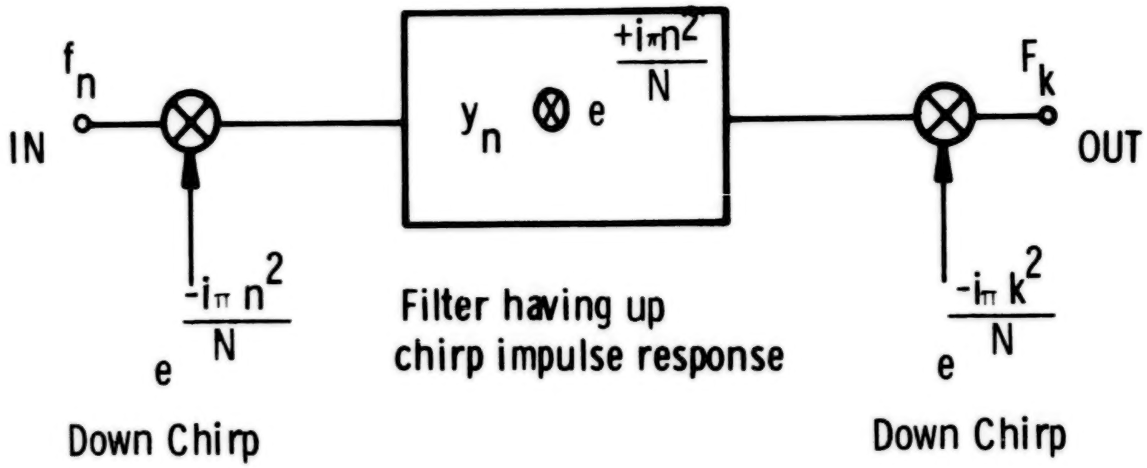

IN
f_n
$e^{\frac{-i\pi n^2}{N}}$
Down Chirp
$y_n \otimes e^{\frac{+i\pi n^2}{N}}$
Filter having up chirp impulse response
F_k
OUT
$e^{\frac{-i\pi k^2}{N}}$
Down Chirp

Figure 2.-Schematic of the CZT Algorithm.

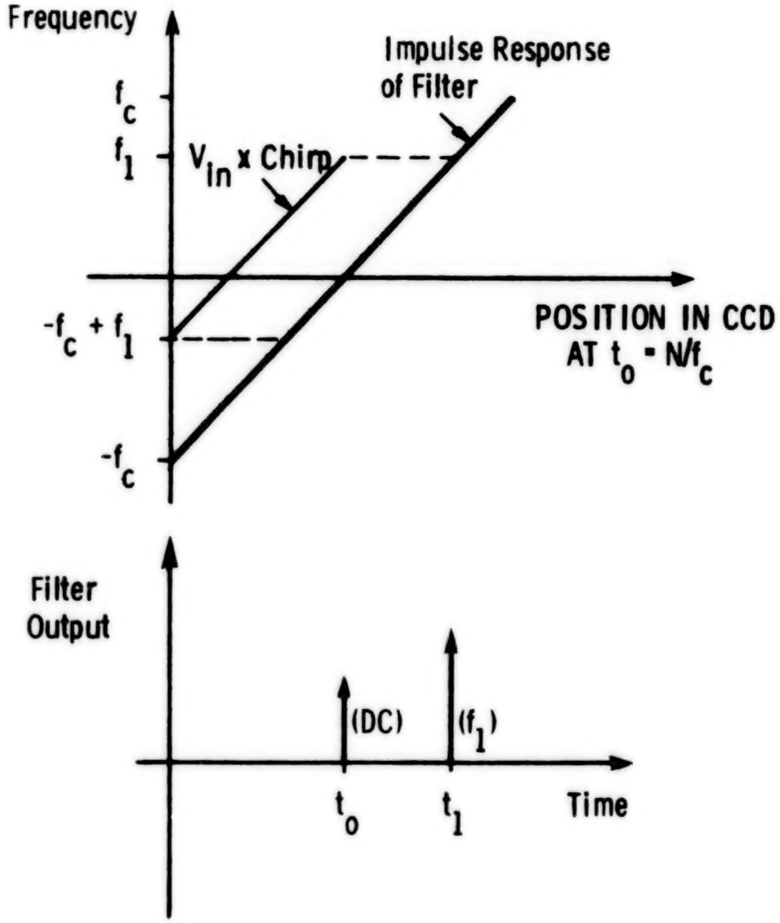

Frequency
Impulse Response of Filter
f_c
f_1
V_{in} x Chirp
$-f_c + f_1$
POSITION IN CCD AT $t_o = N/f_c$
$-f_c$
Filter Output
(DC)
(f_1)
t_o
t_1
Time

Figure 3.-Interpretation of the CZT in Terms of Chirp Input Waveforms in Chirp Filters.

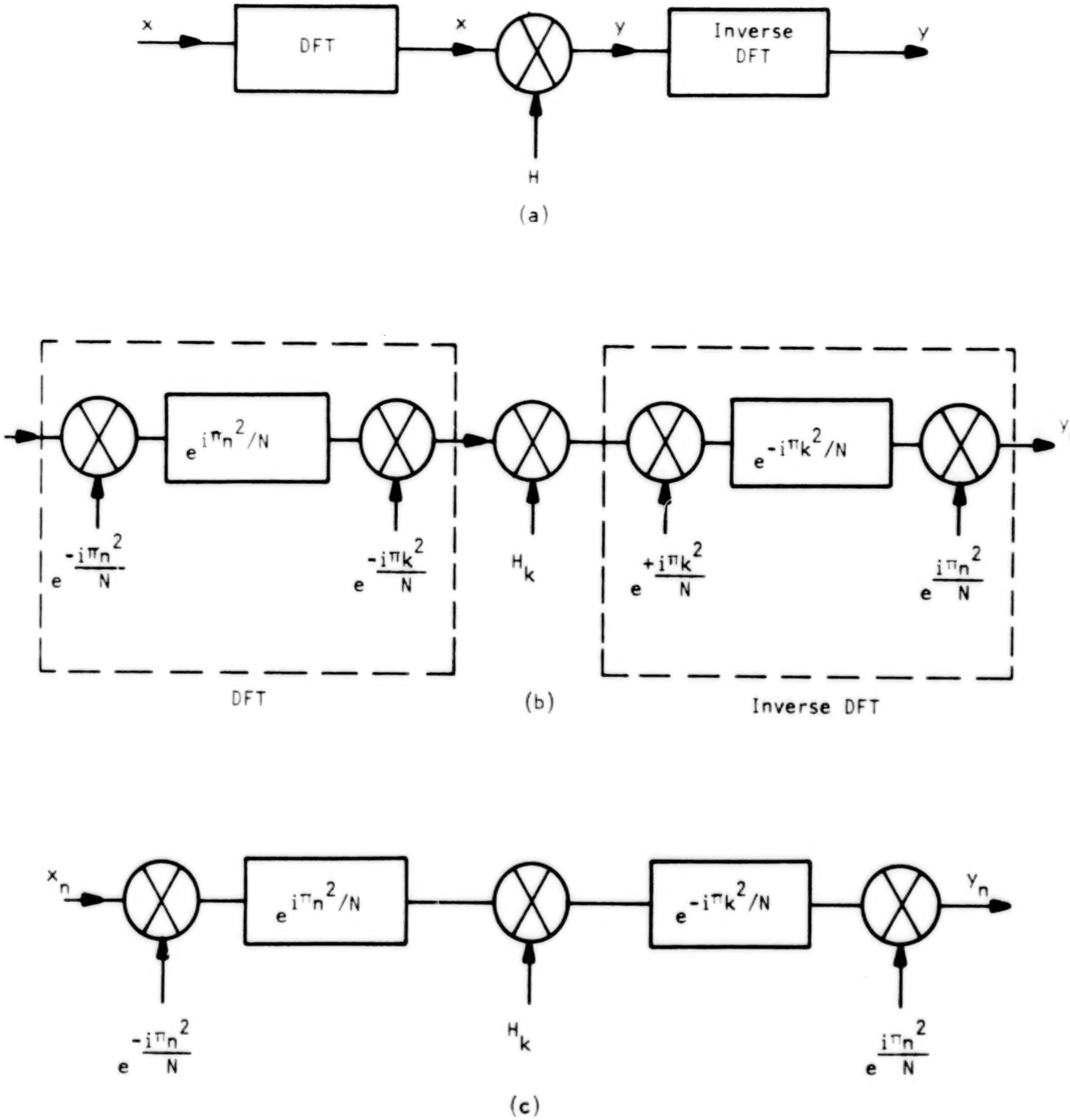

x
DFT
x
y
Inverse DFT
y
H
(a)
x_n
e^{iπn²/N}
e^{-iπn²/N}
e^{-iπk²/N}
H_k
e^{+iπk²/N}
e^{-iπk²/N}
e^{iπn²/N}
y_n
DFT
(b)
Inverse DFT
x_n
e^{iπn²/N}
e^{-iπn²/N}
H_k
e^{-iπk²/N}
e^{iπn²/N}
y_n
(c)

Figure 4.- Block Diagram of a CCD Programmable Correlator.

Figure 4(b) is obtained from 4(a) by replacing the DFT and inverse DFT blocks with their CCD CZT equivalents, and 4(c) is obtained by simplifying 4(b). Figure 4(c), therefore, represents an economical and useful way to perform programmable correlation in pattern classification machines, and this program had as one of its goals the development of CCD CZT ICs to perform spectral analysis for a broad range of NASA requirements including programmable correlation.

The 32-point CCD CZT IC developed under this program is discussed in Section II.

B. Time Domain Correlation

An alternate approach to achieving programmable correlation is the direct time domain correlator. The analog/analog correlator is illustrated in Figure 5.[7] It is similar in operation to the transversal filter illustrated in Figure 1, except that the weighting coefficients are electronically programmable by clocking an analog reference signal into the device. It operates by first loading CCD1 with a reference signal and then clocking a second signal through CCD2. Since the charge is stored dynamically in CCD1, it decays due to thermal leakage and must be refreshed after 10 ms to 100 ms.

Each stage of the CCD is tapped with a diffusion whose potential takes on a value approximately proportional to the signal charge, and four-quadrant multiplication is accomplished using the circuit of Figure 6. Transistors Q_3 and Q_4 act as voltage-controlled resistors, and the balanced configuration overcomes the inherent nonlinearity of MOS transistors used as resistors. The output V_2 from CCD2 is applied to the gate of Q_4, and the gate of Q_3 is biased to V_{ref}, which is equal to the value of V_2 when CCD_2 has the zero level of charge (half-full well). The output from CCD1 is buffered by a source-follower whose output V_a is applied to the drain of Q_3 and Q_4. The sources of Q_3 and Q_4 are connected to virtual ground current buses Σ^- and Σ^+ whose currents are differenced in an off-chip differential amplifier.

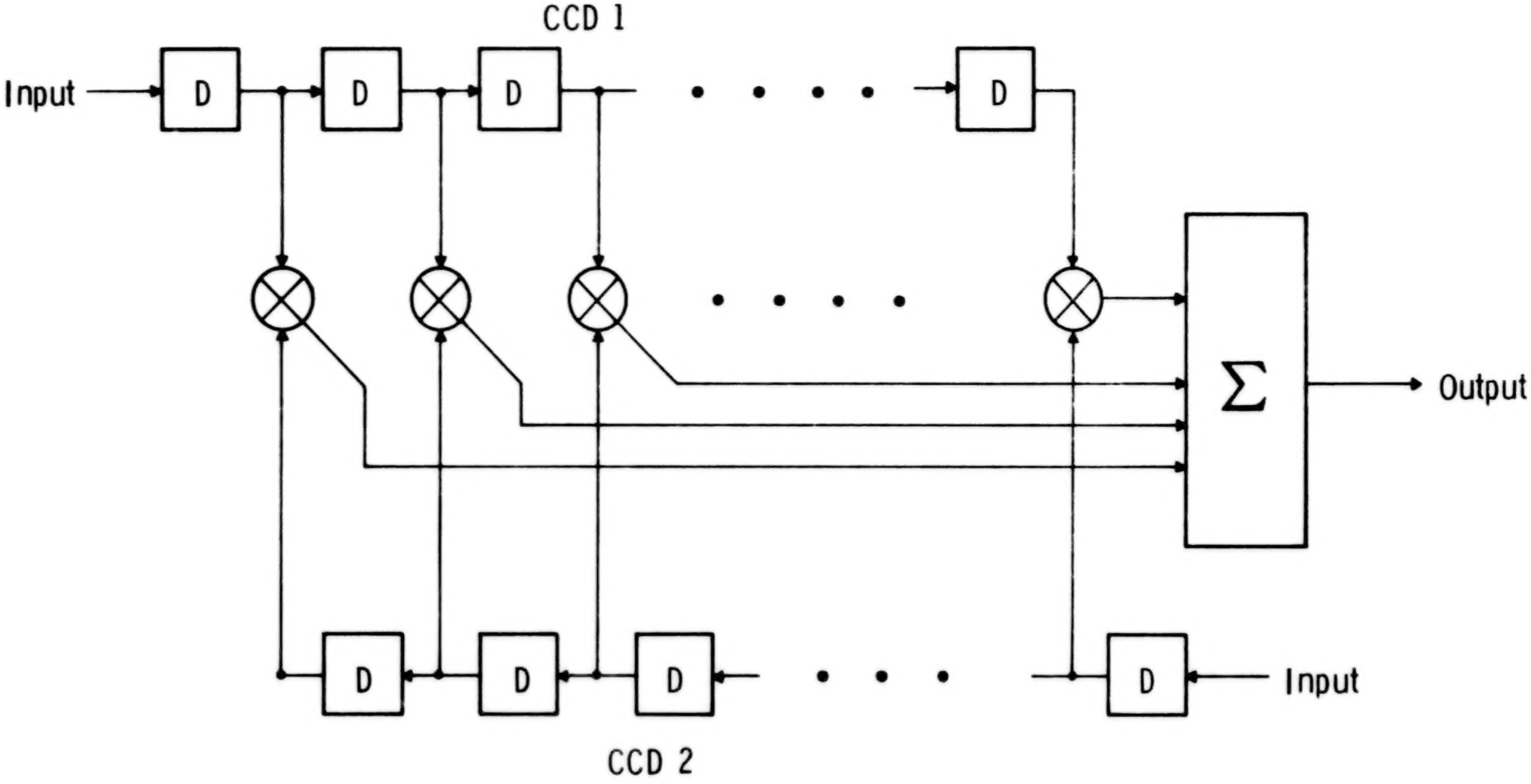

CCD 1
Input
D
D
D
D
Σ
Output
D
D
D
D
Input
CCD 2

Figure 5.-Block Diagram of the Analog/Analog Time Domain Correlator.

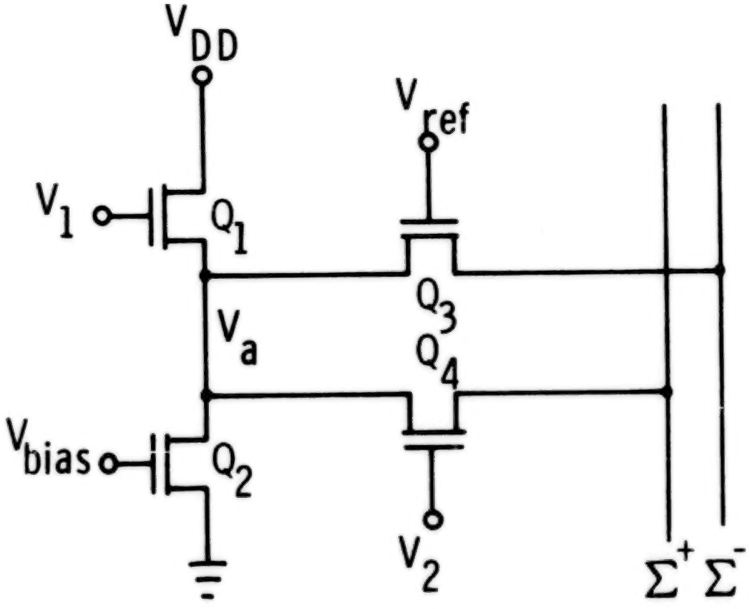

V_{DD}
V_{ref}
V_1
Q_1
V_a
Q_3
Q_4
V_{bias}
Q_2
V_2
Σ^+
Σ^-

Figure 6.-Circuit Schematic of the Four-Quadrant Multiplier Used in the Analog/Analog Correlator of Figure 5.

The currents flowing in Q_3 and Q_4 are

$$I_3 = \beta(V_{ref} - V_t - \tfrac{1}{2}V_a)\,V_a \quad , \tag{5}$$

and

$$I_4 = \beta(V_2 - V_t - \tfrac{1}{2}V_a)\,V_a \quad . \tag{6}$$

The difference current

$$I_4 - I_3 = \beta(V_2 - V_{ref})\,V_a \tag{7}$$

contains no nonlinear terms.

The 64-point analog/analog time domain correlator designed, fabricated, and tested under this contract is discussed in detail in Section III.

An alternate approach to the analog/analog correlator is the binary/analog correlator. The concept of the binary/analog correlator is illustrated in Figure 7. The weighting coefficients ($h_o h_i \ldots h_{N-1}$ of Figure 1) are made electronically programmable by decomposing each one into a binary representation. h_n is represented with M-bit accuracy by

$$h_n = \sum_{k=0}^{M-1} h_n^k\, 2^{-k} \quad . \tag{8}$$

For M-bit accuracy, M parallel CCD binary/analog correlators are put on a chip as shown in Figure 7. The most significant bit h_n^o of each coefficient is loaded into the static shift register (coefficient store) shown as elongated rectangles in the filter at the top of the figure. The second most significant bit h_n^1 of each coefficient is loaded into the second coefficient store, and the least significant bit h_n^{M-1} is loaded into the coefficient store shown at the bottom of the figure. The analog input signal to be filtered is applied without

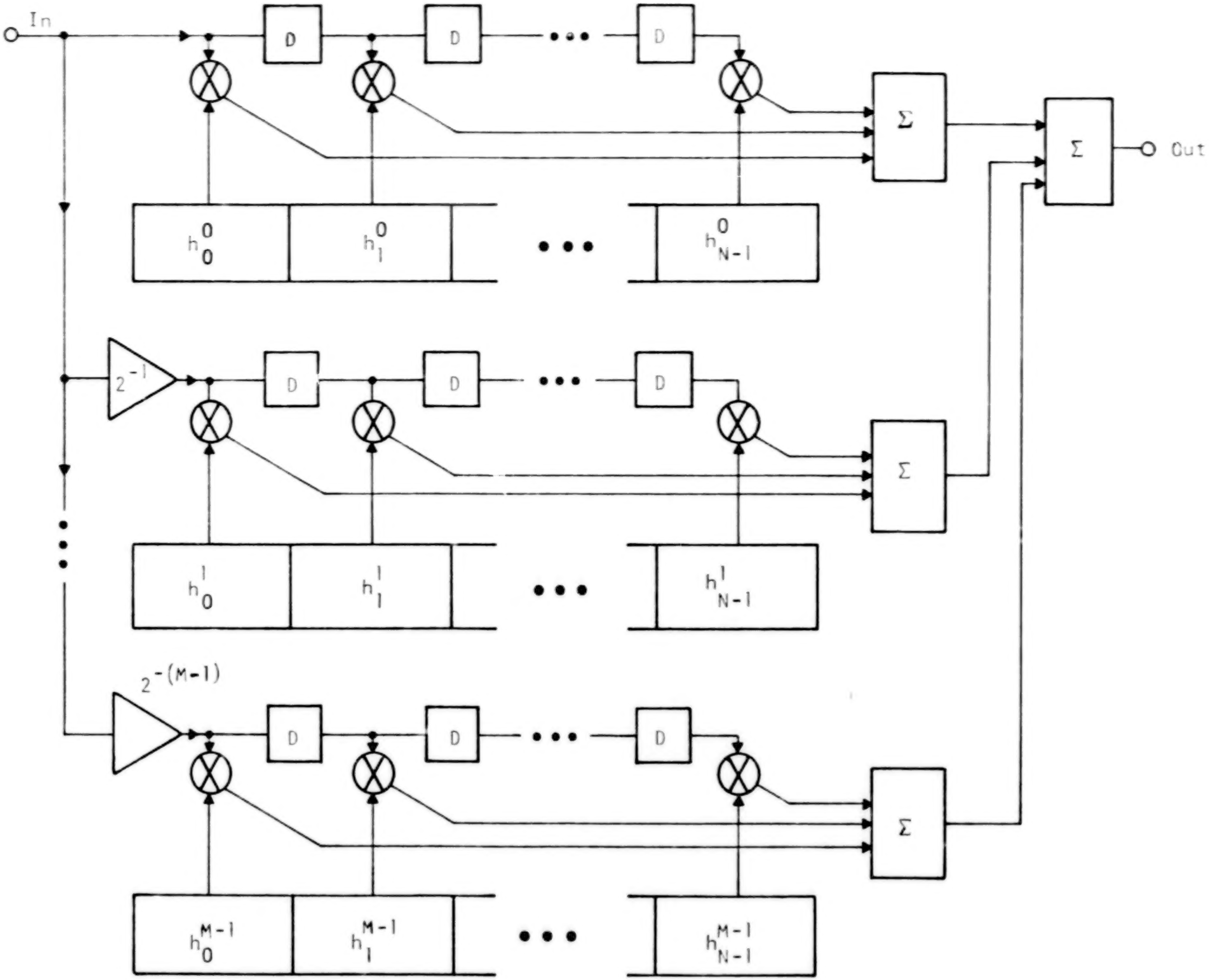

In
D
D
D
Σ
Σ
Out
h_0^0
h_1^0
h_{N-1}^0
2^{-1}
D
D
D
Σ
h_0^1
h_1^1
h_{N-1}^1
$2^{-(M-1)}$
D
D
D
Σ
h_0^{M-1}
h_1^{M-1}
h_{N-1}^{M-1}

Figure 7.- Block Diagram of the Binary/Analog Correlator.

attenuation to the top filter (most significant bit). The input is attenuated by a factor of two at the input of the second filter (second most significant bit), and it is attenuated by a factor of 2^{M-1} at the input to the bottom filter (least significant bit). This attenuation is performed using capacitive ratio techniques similar to those employed in MOS MDAC technology. The coefficients stored in the static shift registers then control the weighting of the transversal filters, and when the outputs of each filter are summed together as shown, the result is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \sum_{n=0}^{N=1} h_n^o Z^{-n} + 2^{-1} \sum_{n=0}^{N-1} h_n^1 z^{-n} + \ldots + 2^{-(M-1)} \sum_{n=0}^{N-1} h_n^{M-1} z^{-n} \quad (9)$$

$$= \sum_{n=0}^{N-1} \left[\sum_{k=0}^{M-1} \left(h_n^k 2^{-k} \right) \right] z^{-n} \quad (10)$$

$$= \sum_{n=0}^{N-1} h_n z^{-n} \quad . \quad (11)$$

The binary/analog correlator is discussed in detail in Section IV.

SECTION II
32-POINT CCD CZT IC

This section describes in detail the design and operation of the frequency domain correlator. The design of each component of the CZT IC is discussed, and applications and experimental results are described.

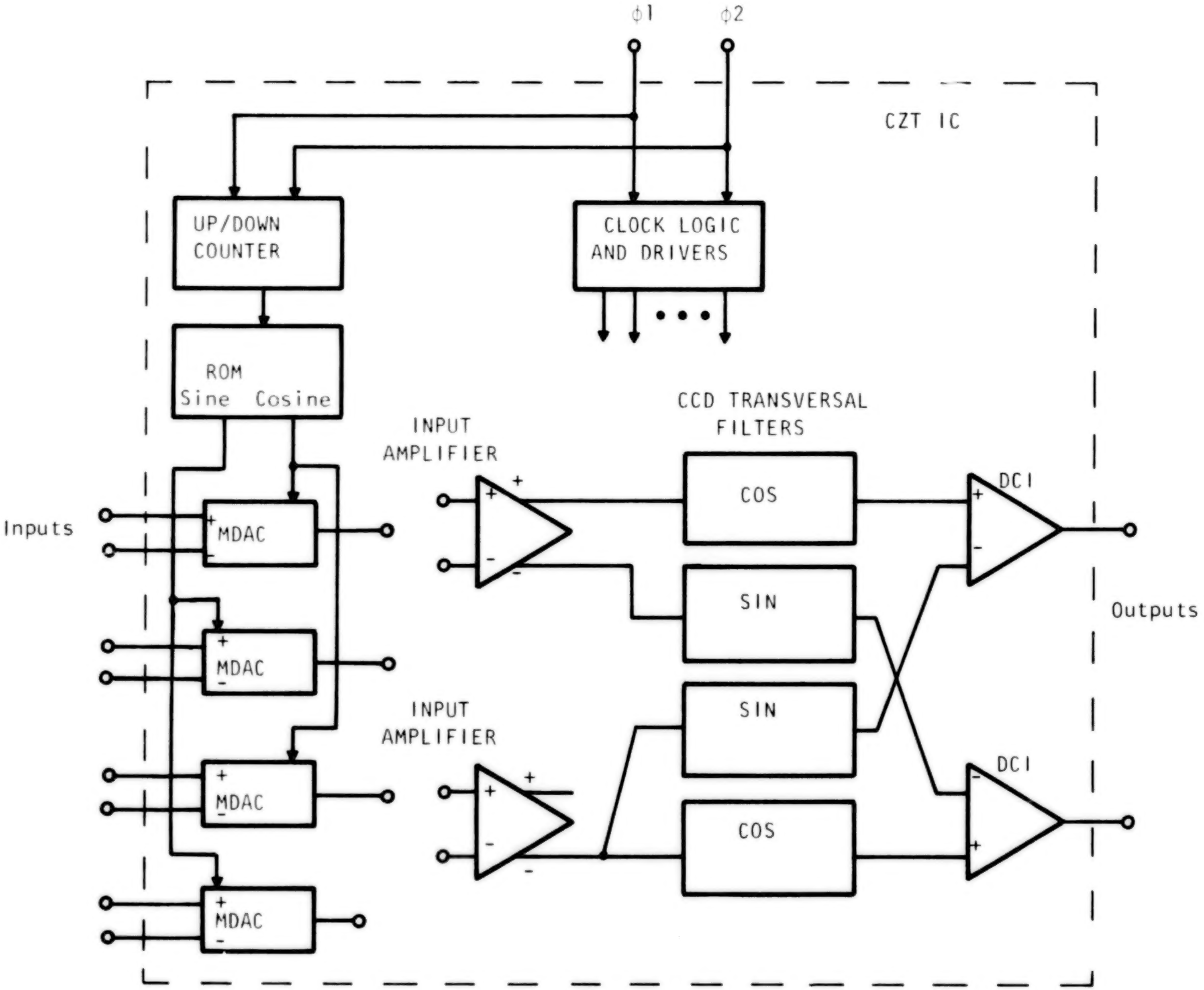
A. Chip Overview

The frequency domain correlator contains all the hardware needed to implement a 32-point CZT, as discussed in the introduction and shown schematically in Figure 4. The IC, shown in block diagram form in Figure 8, is composed of the following:

- ROM
- Up/down counter
- Four MDACs
- Four operational amplifiers
- Eight output buffers
- Clock generators
- Four 64-stage CCD filters.

A photomicrograph of the IC is shown in Figure 9.

The IC measures 6.04 x 5.69 mm^2 (238 x 224 mils^2) and was fabricated using TI's two-phase silicon gate coplanar electrode structure, shown in Figure 10. To provide storage and directionality, n-type ion implants (wells) are diffused under the two clock electrodes. As seen in Figure 10, when both the ϕ_1 and ϕ_2 clocks are off, charge (signal) resides in the wells (under the ϕ_1 electrode for this example). When ϕ_2 is turned on, a potential energy gradient is formed, forcing the charge to move under the ϕ_2 electrode. Next, both clocks are turned off, and the charge remains in the ϕ_2 well. When ϕ_1 is turned on, the charge moves under the ϕ_1 electrode and has moved one bit down the CCD structure.



$\phi 1$
$\phi 2$
CZT IC
UP/DOWN COUNTER
CLOCK LOGIC AND DRIVERS
ROM
Sine
Cosine
CCD TRANSVERSAL FILTERS
INPUT AMPLIFIER
Inputs
MDAC
MDAC
MDAC
MDAC
COS
SIN
SIN
COS
INPUT AMPLIFIER
DCI
DCI
Outputs

Figure 8.-Block Diagram of 32-Point CZT IC.

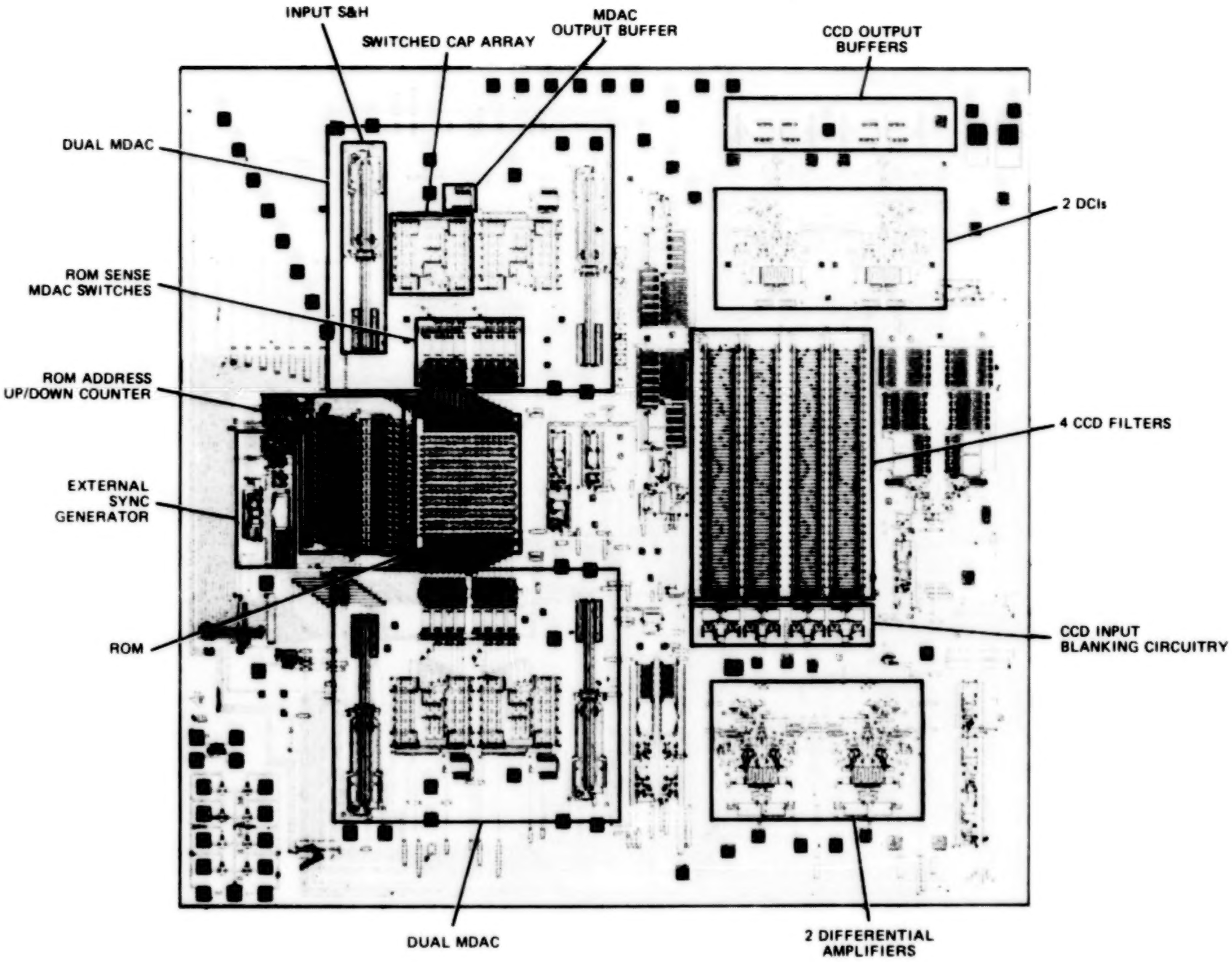

INPUT S&H
SWITCHED CAP ARRAY
MDAC OUTPUT BUFFER
CCD OUTPUT BUFFERS
DUAL MDAC
2 DCIs
ROM SENSE MDAC SWITCHES
ROM ADDRESS UP/DOWN COUNTER
4 CCD FILTERS
EXTERNAL SYNC GENERATOR
ROM
CCD INPUT BLANKING CIRCUITRY
DUAL MDAC
2 DIFFERENTIAL AMPLIFIERS

Figure 9.-Photomicrograph of 32-Point CCD CZT IC.

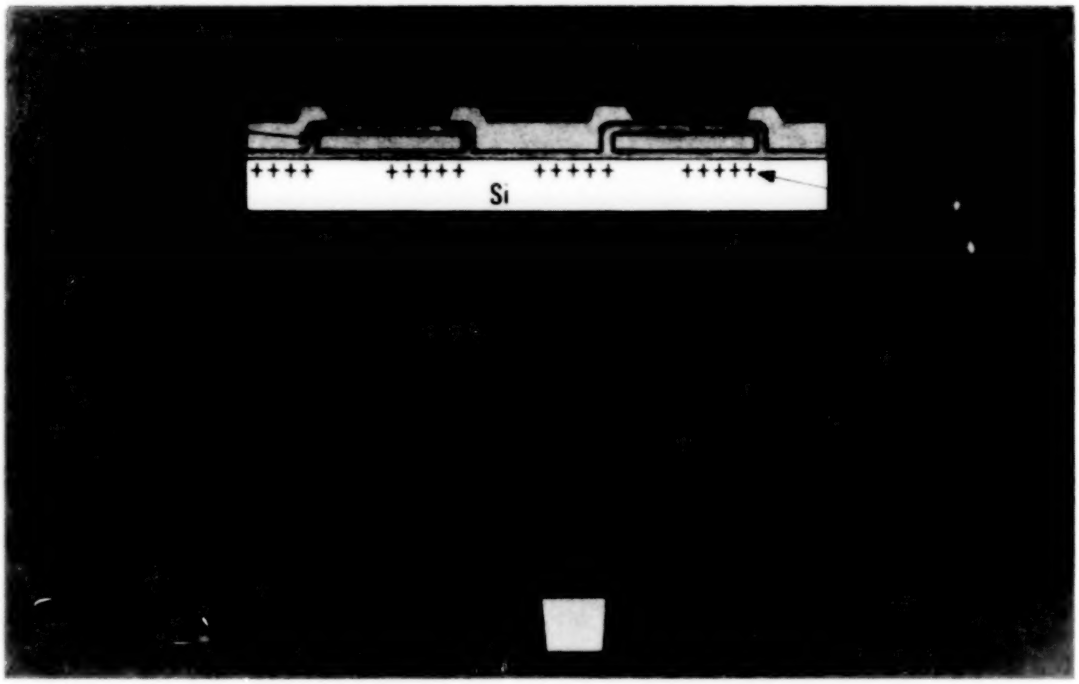
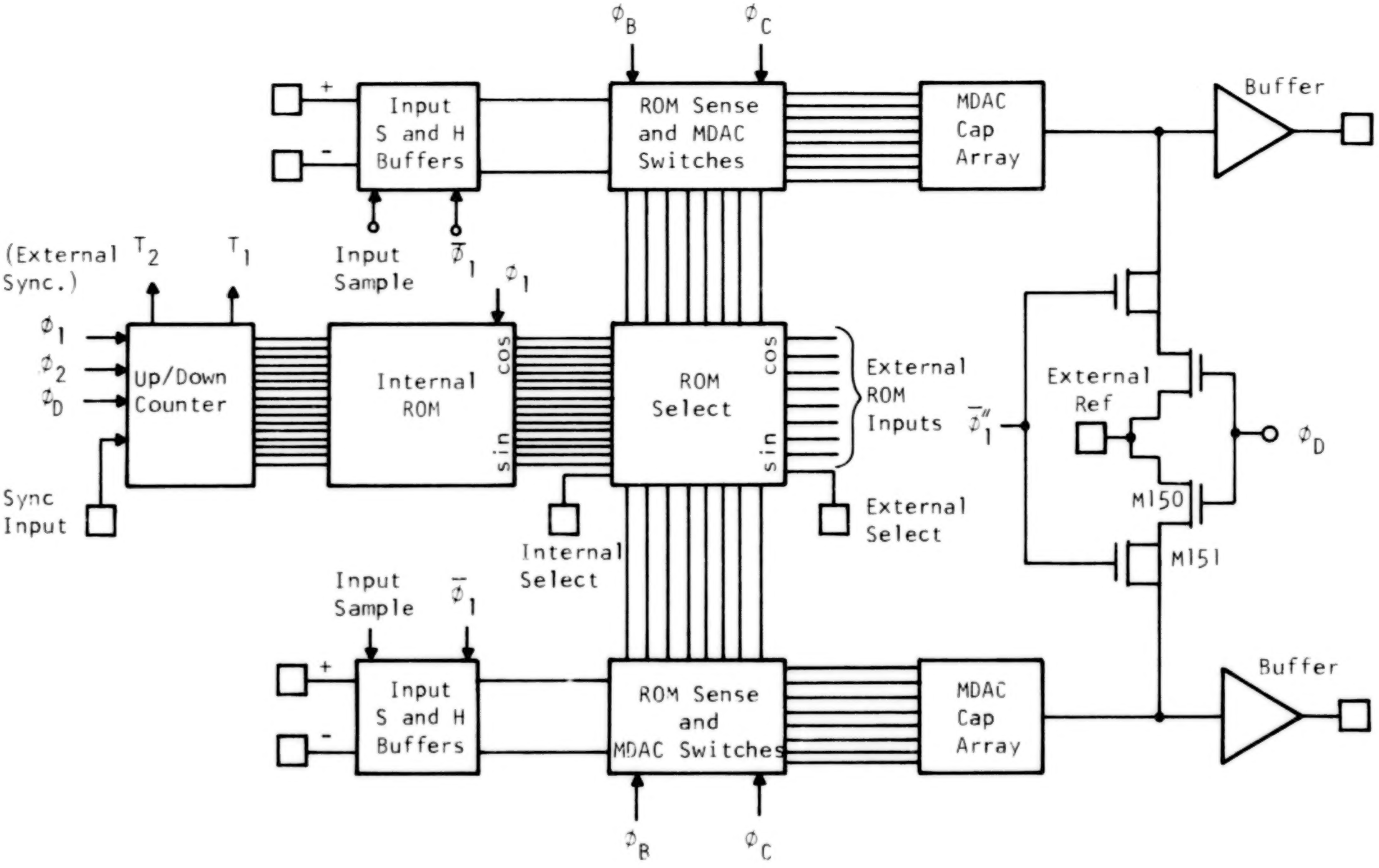


Figure 10.-Silicon Gate CCD Coplanar Electrode Structure.

Because of the complexity of the analog circuits surrounding the CCD filters, much circuit modeling and MOSFET modeling was needed. To obtain accurate MOSFET models for use in the circuit modeling, data were taken on MOSFETs from previously processed ICs. These data were tabulated and fitted to the Shichman-Hodges MOS equations using the computer, and parameter values were extracted for circuit modeling. This procedure allowed the design of the peripheral circuitry to be accomplished with a high degree of confidence.

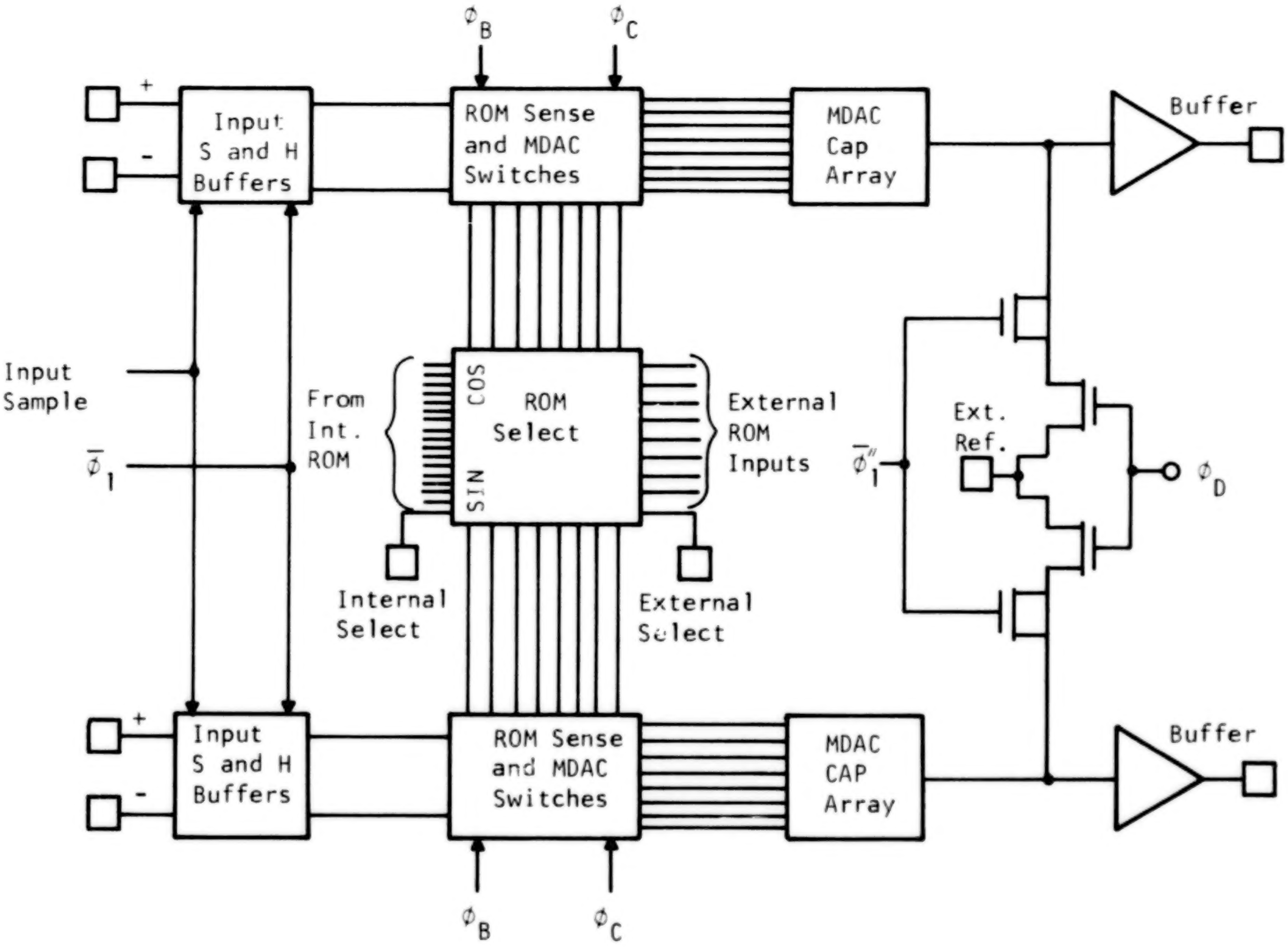
In an effort to provide the greatest possible flexibility, the IC was partitioned into three main signal processing sections. The first two sections are both dual MDACs. The MDACs and their associated circuitry are shown in Figures 11 and 12. The ROM is common to both sets of MDACs and has 16 output lines, 8 for the sin chirp words and 8 for the cosine chirp words. The sin chirp is available to one MDAC in each figure, and the cos chirp is available to the other two MDACs. The eight-bit external word is available to all four MDACs and may be individually selected for each set of dual MDACs. Each MDAC consists of an input sample-and-hold buffer, ROM sense and MDAC drive circuitry, the MDAC capacitor array, and an output buffer. The third section of the partition, shown in Figure 13, consists of two CCD input amplifiers (A_1 and A_2), CCD input blanking circuitry, four 64-stage CCD transversal filters, two differential current integrators (CCD output amplifiers), and four output buffers. The CCD input amplifiers make the inverse of the signal available to the CCDs so that both CCD outputs to the DCI may be summed the same way. The CCD input blanking circuitry uses the T_1 and T_2 pulses from the up/down counter to load "zeros" into the CCD for appropriate periods. The T_2 pulse is always used. The T_1 pulse is used only to implement the noncircular correlation function and must be stitch-bonded on-chip if it is required.

Each of the three partitioned sections utilizes output buffering circuits so that the sections can be connected in several configurations using one or more ICs. Also, each section has the circuitry required to process real and



ϕB
ϕC
Input
S and H
Buffers
ROM Sense
and MDAC
Switches
MDAC
Cap
Array
Buffer
+
-
(External
Sync.)
T2
T1
Input
Sample
ϕ̄1
ϕ1
ϕ1
ϕ2
ϕD
Up/Down
Counter
Internal
ROM
cos
sin
ROM
Select
cos
sin
External
ROM
Inputs
ϕ̄″1
External
Ref
ϕD
M150
M151
Sync
Input
Internal
Select
External
Select
Input
Sample
ϕ̄1
Input
S and H
Buffers
ROM Sense
and
MDAC Switches
MDAC
Cap
Array
Buffer
+
-
ϕB
ϕC

Figure 11.-Block Diagram of Internal ROM, Up/Down Counter, and Dual MDACs.



ϕB
ϕC
+
-
Input S and H Buffers
ROM Sense and MDAC Switches
MDAC Cap Array
Buffer
Input Sample
ϕ̄1
From Int. ROM
COS
ROM Select
SIN
External ROM Inputs
Internal Select
External Select
Ext. Ref.
ϕ̄″1
ϕD
+
-
Input S and H Buffers
ROM Sense and MDAC Switches
MDAC CAP Array
Buffer
ϕB
ϕC

Figure 12.-Block Diagram of Second Dual MDAC.

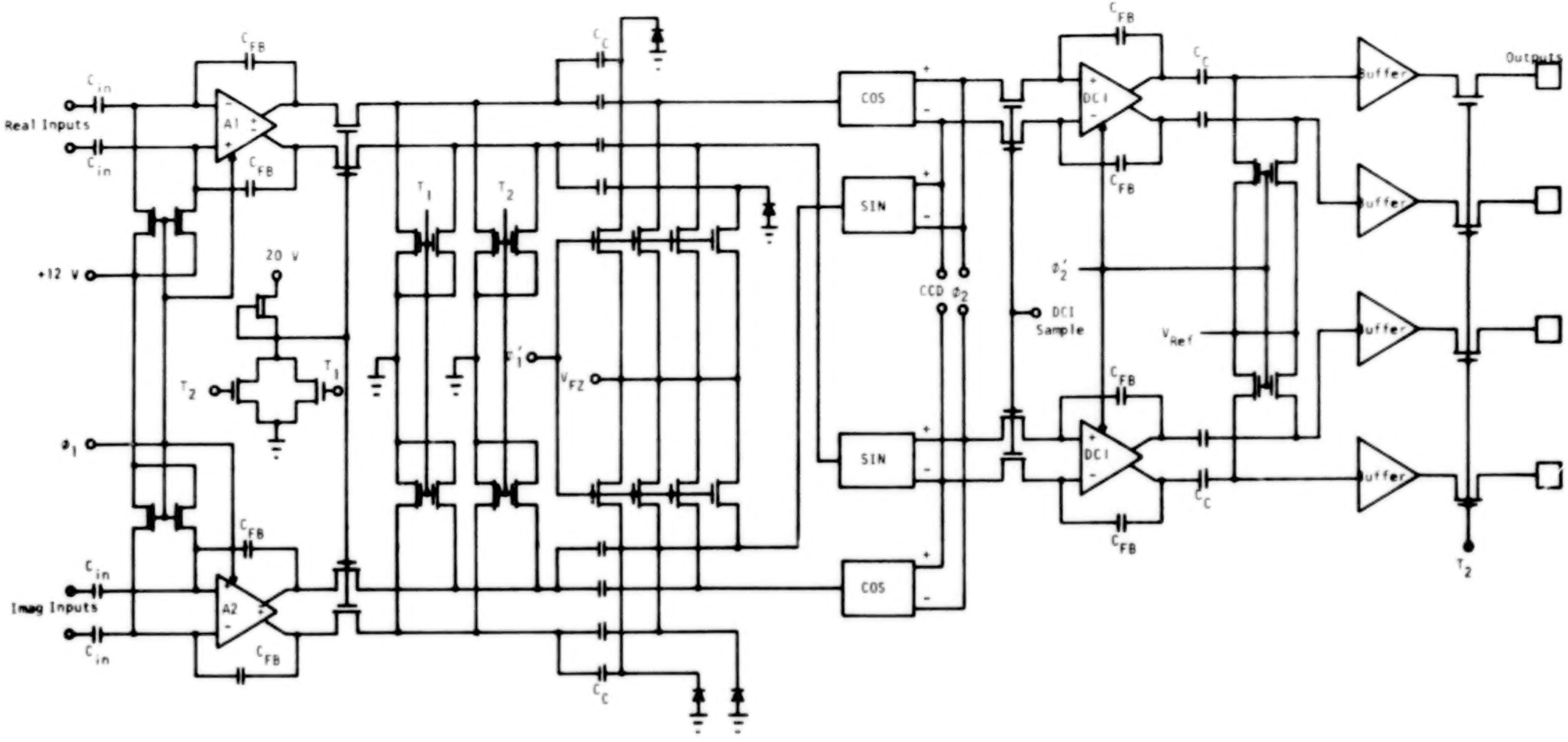

C_{in}
Real Inputs
C_{in}
C_{FB}
A1
C_{FB}
+12 V
20 V
T_2
T_1
ϕ_1
C_{FB}
C_{in}
Imag Inputs
A2
C_{in}
C_{FB}
C_C
T_1
T_2
ϕ_1'
V_{FZ}
C_C
COS
SIN
SIN
COS
CCD ϕ_2
DCI Sample
C_{FB}
DCI
C_{FB}
ϕ_2'
V_{Ref}
C_{FB}
DCI
C_{FB}
C_C
C_C
Buffer
Buffer
Buffer
Buffer
Outputs
T_2

Figure 13.- Block Diagram of CCD Input Amplifiers, CCDs, DCI, and Output Buffers.

imaginary signal components. In addition to the three partitioned sections described above, the chip contains clock-generating circuitry. The clock generators derive all the internal timing pulses from the two-phase clocks input to the IC.

B. CCD Filter

The four filters needed to implement the CZT algorithm are chirp convolution filters with 2N-1 stages. A photograph of the four CCD filters is shown in Figure 14. The weighting coefficients for the sine and cosine chirp filters are

$$h_k^{\cos} = \cos \frac{\pi k^2}{32} \qquad k = 0,31$$

$$h_k^{\sin} = \sin \frac{\pi k^2}{32} \qquad k = 0,31 \quad .$$

The coefficients were realized using the split-electrode technique, and because the CZT IC was designed to perform the true CZT, the filter tapweights were repeated for the remaining N-1 stages of the filters.

The CCD filter structure is illustrated in Figure 15. Each filter is surface channel and uses two-phase clocking. Each stage is 25.4 μm (1 mil) long and consists of a 12.7 μm (0.5 mil) long first poly electrode and a second poly electrode that is effectively 12.7 μm (0.5 mil) long. The barriers are 5.1 μm (0.2 mil) each, and the wells are 7.6 μm (0.3 mil) each. The channel width is 155 μm (6.1 mils). The split electrodes are the first poly electrodes. The split electrode gaps are 5 μm (0.2 mil), and the channel stop beneath each gap is 12.7 μm (0.5 mil) wide.

The channel stop beneath each gap serves two purposes. The first is to prevent the electrons of the signal charge packets from being trapped in these

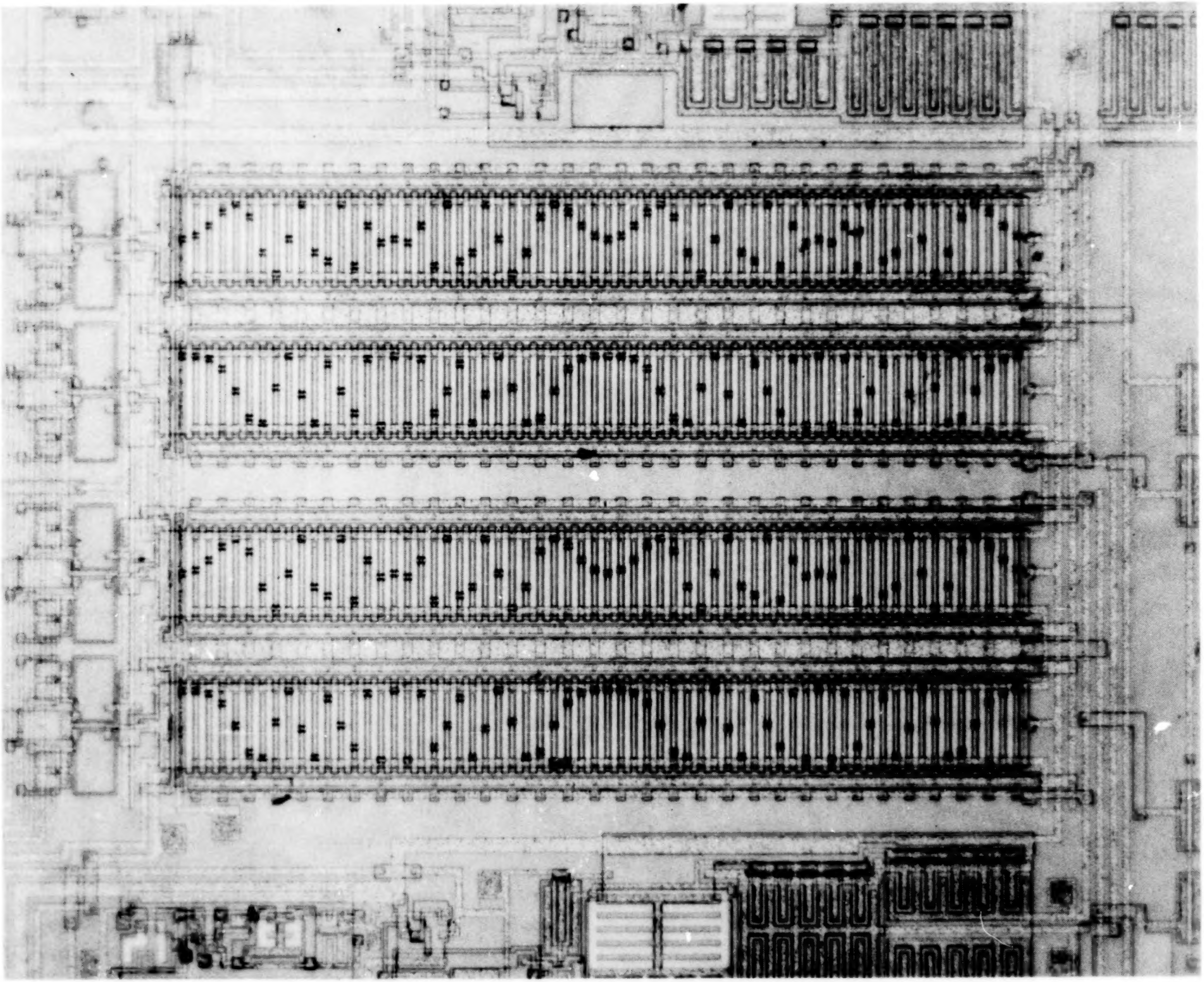


Figure 14.-Photomicrograph of CCD Transversal Filters.

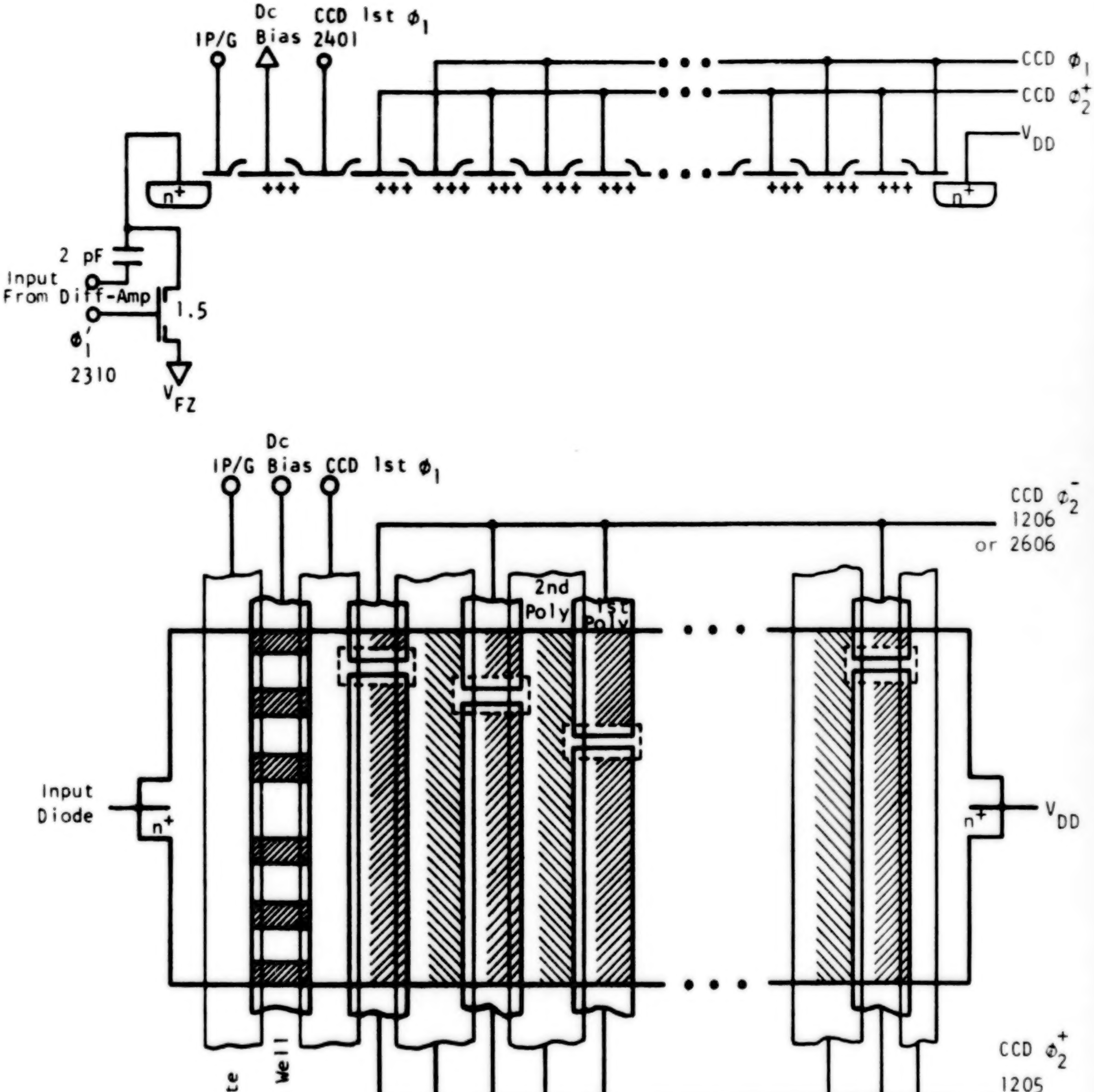

IP/G
Dc Bias
CCD 1st ϕ_1 2401
CCD ϕ_1
CCD ϕ_2^+
V_{DD}
n^+
+++
2 pF
Input From Diff-Amp
1.5
ϕ_1'
2310
V_{FZ}
IP/G
Dc Bias
CCD 1st ϕ_1
CCD ϕ_2^- 1206 or 2606
2nd Poly
1st Poly
Input Diode
n^+
V_{DD}
Input Gate
Receiving Well
CCD ϕ_2^+ 1205 or 2605
CCD ϕ_1 1507

Figure 15.-Schematic of CCD Filters.

areas and causing serious degradation of the charge transfer efficiency. The second reason for the channel stop is that the position of the weighting coefficients is defined by the same photomask that defines the CCD channel. Thus, the weighting coefficient accuracy is determined by the accuracy with which the photomask is made and is not dependent on alignment of different photomask levels in the device fabrication process. With this approach approximately 0.16% accuracy in the weighting coefficients is possible with a 155 μm (6.1 mil) wide channel in the CCD. This gives an area for the first well area of $7.6 \times (1.55 - 12.7) = 1084\ \mu m^2$ $[0.3 \times (6.1 - 0.5) = 1.68\ mil^2]$.

The CCD clocking sequence is illustrated in Figure 16 relative to the two-phase input clocks ϕ_1 and ϕ_2. The analog input to the CCD is capacitively coupled to the input diode. The fat-zero level on the diode is set to V_{FZ} when ϕ_1' comes up. After ϕ_1' falls, the CCD input signal is allowed to change and the IP/G signal pulls up, dumping signal charge into the receiving well, which is controlled by a dc bias. The total receiving well area is $710\ \mu m^2$ $(1.1\ mil^2)$, making the capacity of this well 65% as large as the capacity of the following wells. This prevents saturation of the filter. The signal is sampled when IP/G falls. Next, the CCD first ϕ_1 clock rises and falls, dumping the sampled signal charge under the first split electrode. The CCD first ϕ_1 electrode rises to a level less than that of the CCD $\phi_2^{\pm}$ clock lines to make sure that all charge is transferred. At the same time, the CCD ϕ_1 electrodes fall, transferring the charge packets under the CCD ϕ_1 electrodes to the remaining split electrodes. These split electrodes must be floating when this occurs in order to sense the charge packets.

The capacitive coupling of the CCD ϕ_1 line to the CCD $\phi_2^{\pm}$ lines is compensated for by another clock, $\overline{CCD\phi_1}$, which is capacitively coupled to the CCD $\phi_2^{\pm}$ lines by approximately the same amount. The $\overline{CCD\phi_1}$ clock comes up when CCD ϕ_1 clock falls. The output signal is sampled before the CCD ϕ_1 line rises

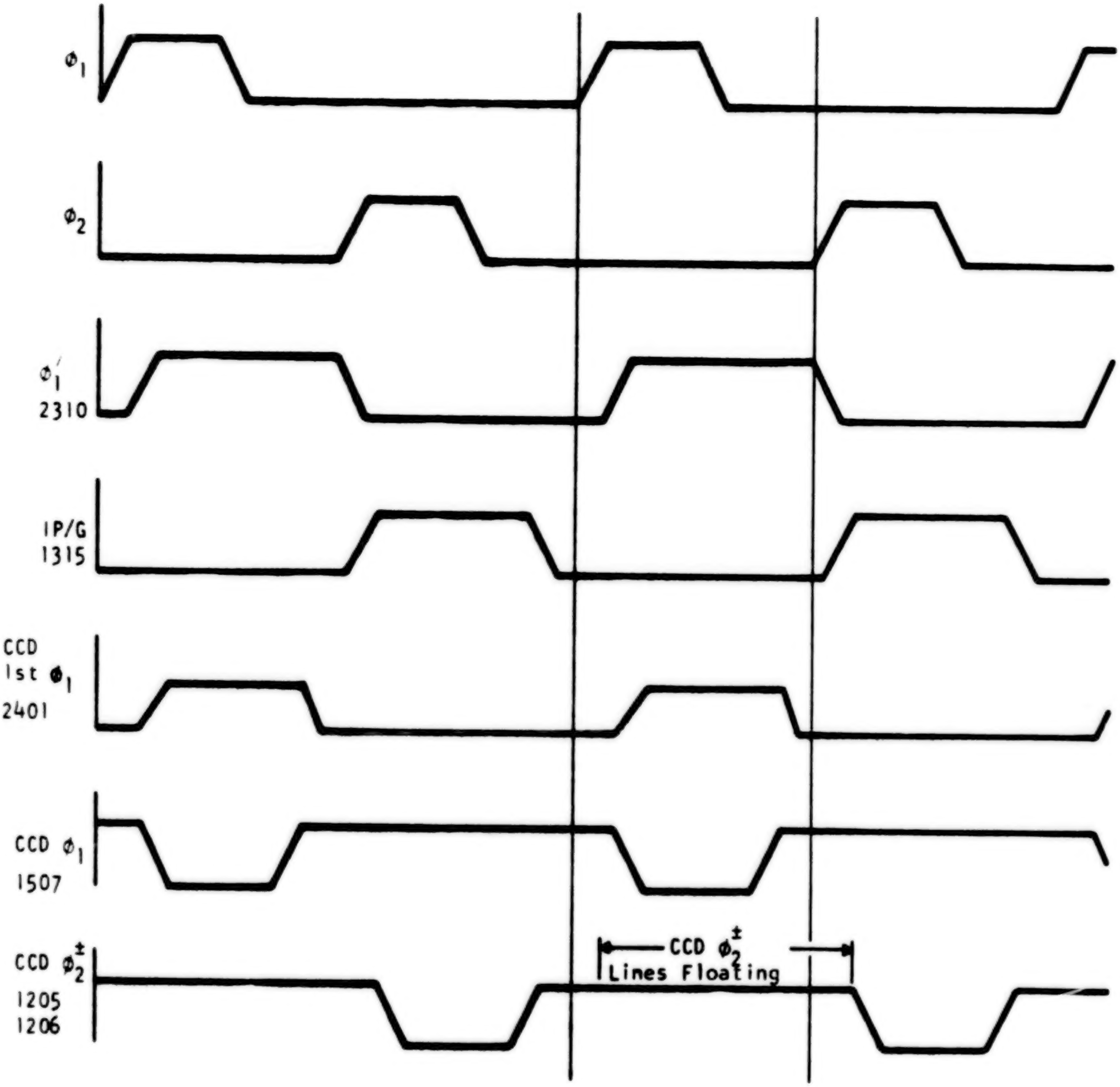

ϕ_1
ϕ_2
ϕ_1'
2310
IP/G
1315
CCD
1st ϕ_1
2401
CCD ϕ_1
1507
CCD $\phi_2^\pm$
1205
1206
CCD $\phi_2^\pm$
Lines Floating

Figure 16. - CCD Timing.

again. When the CCD $\phi_2^{\pm}$ electrodes are pulled down, the charge packets are transferred to the following CCD ϕ_1 electrodes. When each charge packet reaches the end of the CCD, it is dumped onto the output diode, which is tied to V_{DD}. An effort was made in laying out the four CCDs and their interconnects to match the capacitance on all four output lines. Consideration was given both to capacitance to the substrate and to capacitance to the other clock lines.

C. Operational Amplifiers

1. Design

In the realization of the 32-point CZT, four operational amplifiers are needed to perform two functions. The first function is to provide gain and the inverse of the signal to the inputs of the CCDs. These amplifiers are called the input diffamps and are designated as A1 and A2 in Figure 13. The need for the inverse of the signal can be understood best by considering the function of the differential current integrator (DCI).

The general DCI scheme and the capacitances associated with the CCD are shown in Figure 17. The following capacitances are indicated in the figure:

C_S = stray to substrate, made equal on $V^{\pm}$ nodes.
C_{OF} = fixed overlaps from phase 1 (ϕ_1) to $V^{\pm}$ nodes, also made equal.
C_{OL} $(1 \pm h_i)/2$ = overlap to ϕ_1 for each stage, depends on h_i.
C_{OF} + N/2 C_{OL} = a coupling to $\overline{\phi_1}$, equal for each node $V^{\pm}$.
C_{OX} $(1 \pm h_i)/2$ = $V^{\pm}$ electrode to channel capacitance for each stage.
C_D $(1 \pm h_i)/2$ = depletion layer capacitance for each stage.

A possible timing scheme is shown in Figure 18. The operation is as follows. The split electrode nodes $V^{\pm}$ are clocked to the voltage V_2 via the series switches S_2, while the phase 1 (ϕ_1) clock is high. The switches S_2 are then turned off, and nodes $V^{\pm}$ are left floating. The next point in the timing

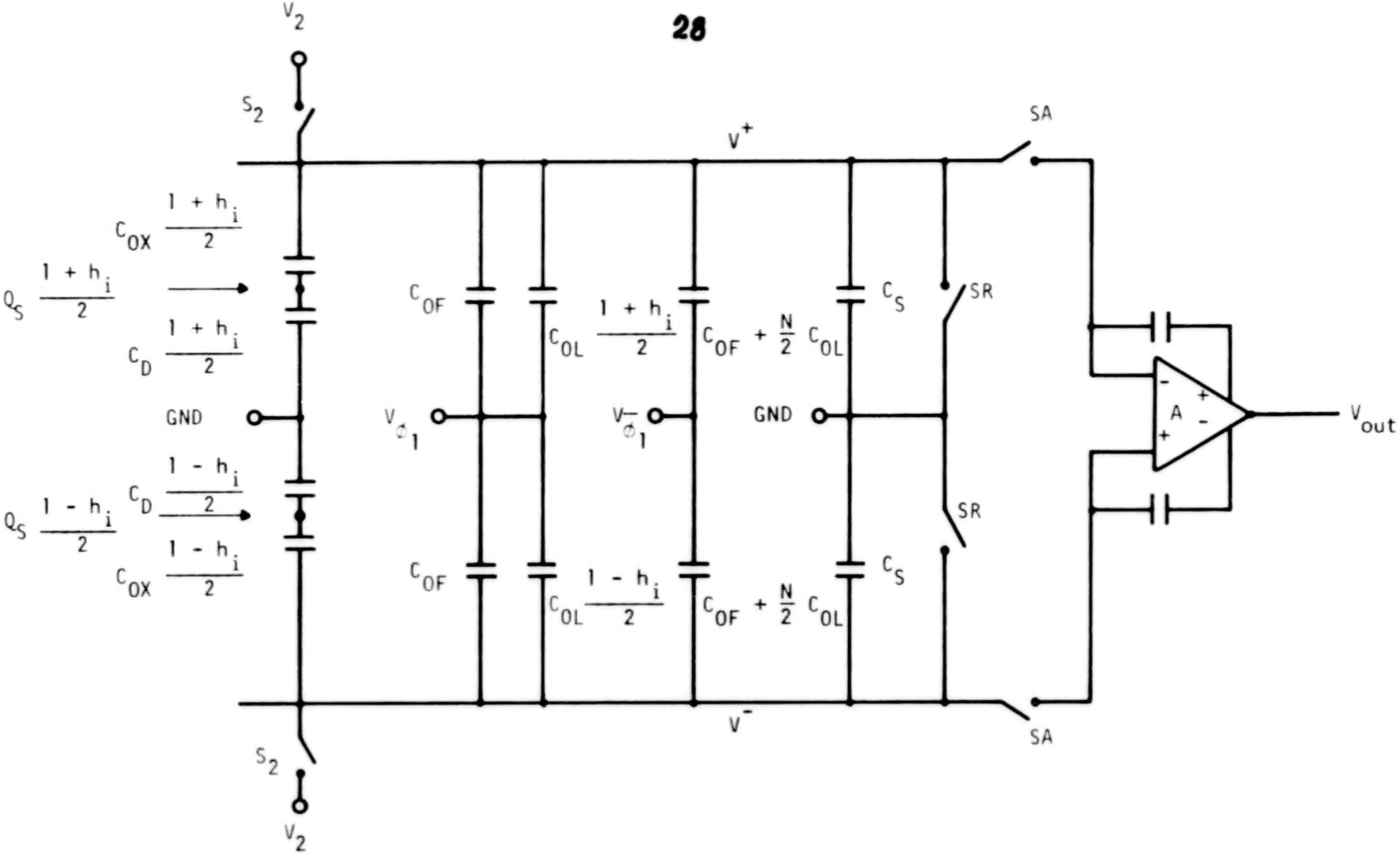

V2
S2
V+
SA
C_OX (1 + h_i)/2
Q_S (1 + h_i)/2
C_D (1 + h_i)/2
C_OF
C_OL (1 + h_i)/2
C_OF + N/2 C_OL
C_S
SR
GND
V_φ1
V_φ̄1
GND
A
V_out
C_D (1 - h_i)/2
Q_S (1 - h_i)/2
C_OX (1 - h_i)/2
SR
C_OF
C_OL (1 - h_i)/2
C_OF + N/2 C_OL
C_S
V-
SA
S2
V2

Figure 17.-CCD Capacitances.

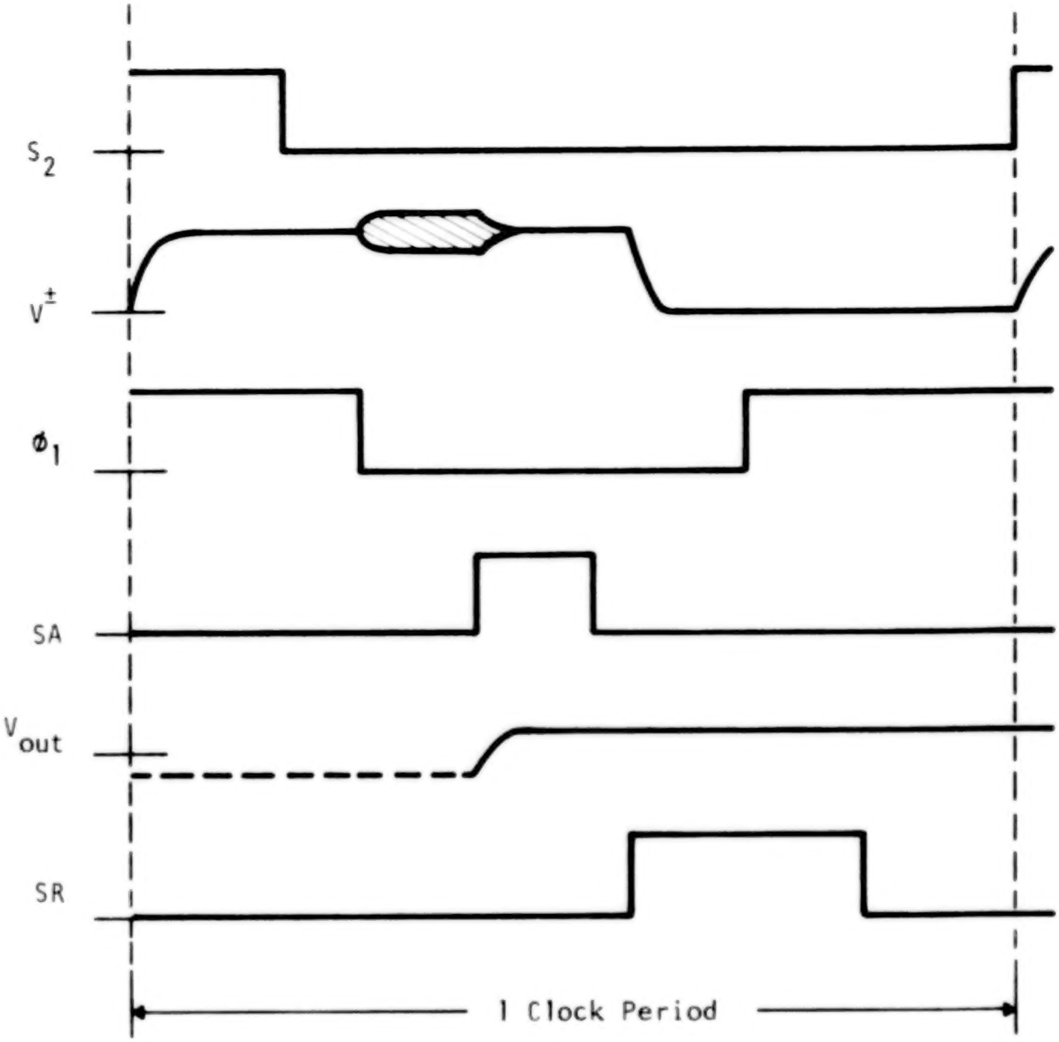

S_2
$V^{\pm}$
ϕ_1
SA
V_{out}
SR
1 Clock Period

Figure 18.-A Possible Switching Diagram for Figure 17. A high voltage on a switch turns it on.

diagram is the turn-off of phase 1. At this point the charge transfers under the split electrodes. The nodes $V^{\pm}$ are isolated, and feedthrough from ϕ_1 via the overlap capacitance could reduce the voltage $V^{\pm} \simeq V_2$ to a value low enough so that incomplete transfer could take place. To prevent this, a capacitive coupling to $\bar{\phi}_1$ is provided, which is approximately equal to the coupling to ϕ_1.

As the signal charge Q_S flows under the split electrodes, the node voltages $V^{\pm}$ change in proportion to the sum of the tap weights $(1 \pm h_i)$. The node voltages then are

$$V^{\pm} = V_2 - V_{\phi_1}\left[C_{OF} + \sum_{i=1}^{N} (1 \pm_h i)\ C_{OL}\right]/2C^{\pm}$$

$$+ V_{\bar{\phi}_1}(C_{OF} + \frac{N}{2} C_{OL})/2C^{\pm} + \sum_{i=1}^{N} C_{OX}(1 \pm h_i)(V_i + V_z)/2C^{\pm} \quad , \qquad (12)$$

where

$$C^{\pm} = C_S + 2C_{OF} + C_{OL}\frac{N}{2}(2 \pm \bar{h}) + C_E\frac{N}{2}(1 \pm \bar{h}) \quad , \qquad (13)$$

and $C_E = C_{OS}$, C_D in series, and

$$\bar{h} = \sum_{i=1}^{N} h_i/N,$$

V_z = bias voltage for zero signal (fat zero),

V_i = signal voltage sampler.

The node voltages $V^{\pm}$ are to be sensed by the differential feedback amplifier A when the switches SA are turned on at the next stage in the timing diagram. The negative feedback of the amplifier causes its output to change until the input voltages V^{+} and V^{-} are equal.

The output voltage V_{out} is proportional to the difference:

$$V^{+} - V^{-} = -V_{\phi_1} N\bar{h} C_{OL}/C + V_z N\bar{h} C_{OX}/C + C_{OX} \sum_{i=1}^{N} h_i V_i/C \quad , \qquad (14)$$

where C^{+} and C^{-} have been made equal by the addition of $(C_{OL} + C_E) N\bar{h}$ to node V^{-}. In practice, the addition may have to be made to V^{+} if $\bar{h}$ is negative.

Only the third term in Equation (14) is the desired output of the convolution filter. The first two terms need to be eliminated. This can be accomplished in two ways. The first involves an additional channel in parallel with the signal channel. This new channel is of width $|\bar{h}| \cdot W_S$ if W_S is the signal channel width, and is located on the side of the V^{-} electrode if $\bar{h} > 0$. The new channel only carries a signal equal to V_z. Again, in practice, two such channels may be required, one on each side of the main signal channel. Their widths are then adjusted so that they differ by $|\bar{h}|\ W_S$. A possible layout of such a structure is shown in Figure 19. The addition not only cancels the two unwanted parts in the output [Equation (14)], but also adds just the required capacitances to equalize C^{+} and C^{-}.

A second way the two additional terms in Equation (14) can be cancelled is appropriate to the chirp z-transform. Here the output of a cos and a sin chirp are added. However, the values of $\bar{h}$ for the sin and cos chirp are equal, at least for an even number of stages. Even when apodization is added to the CCD chirp filter, as may be done for a sliding transform, the values of $\bar{h}$ differ by only a small amount. For example, for even N, $\bar{h}(\cos) = \bar{h}(\sin) = 1/\sqrt{2N}$. For a Hamming weighted filter we calculate

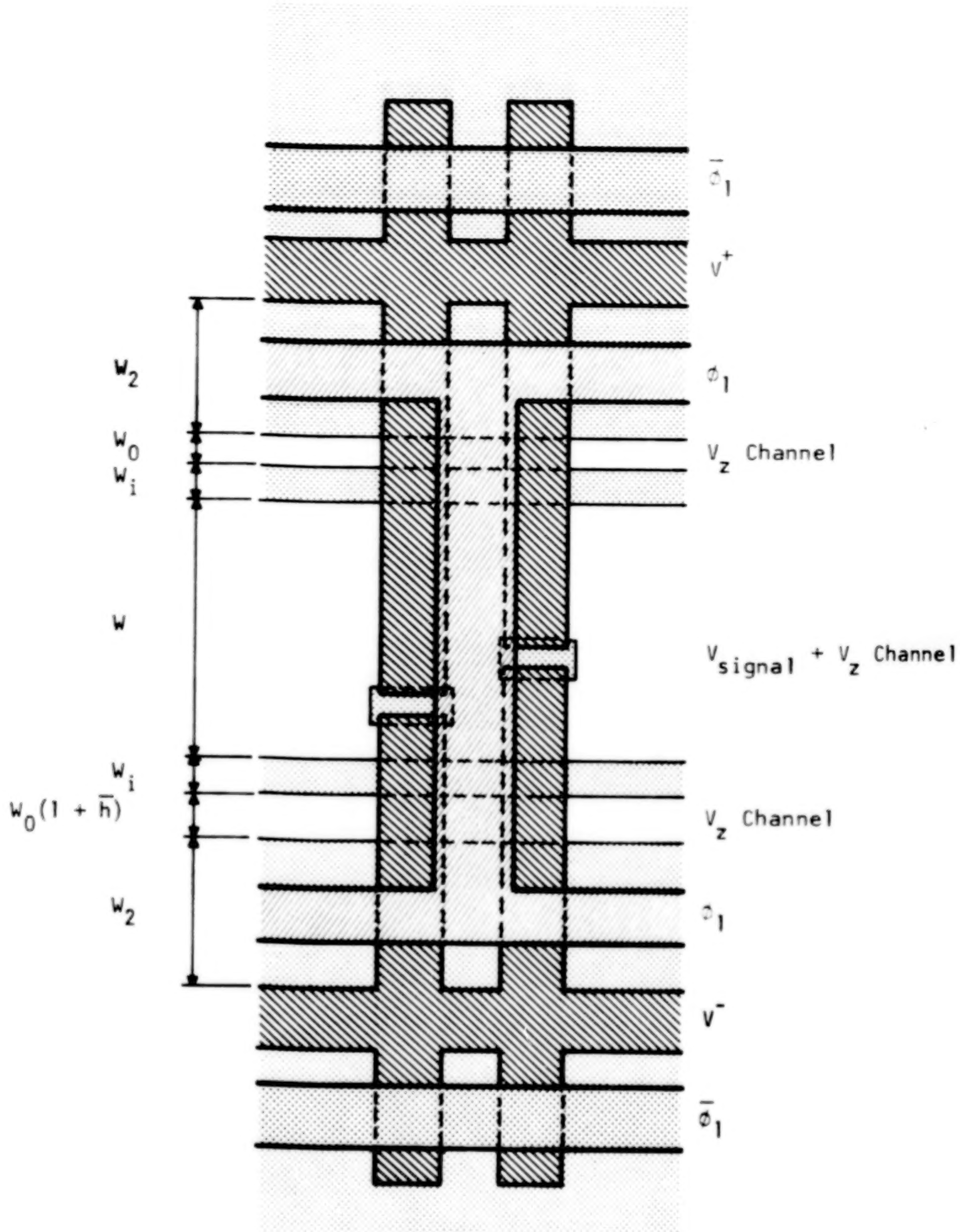

$\bar{\phi}_1$
V^+
W_2
ϕ_1
W_0
W_i
V_z Channel
W
$V_{signal} + V_z$ Channel
W_i
$W_0(1 + \bar{h})$
V_z Channel
W_2
ϕ_1
V^-
$\bar{\phi}_1$

Figure 19.- Symmetrized and Compensated Two-Phase CCD Layout.

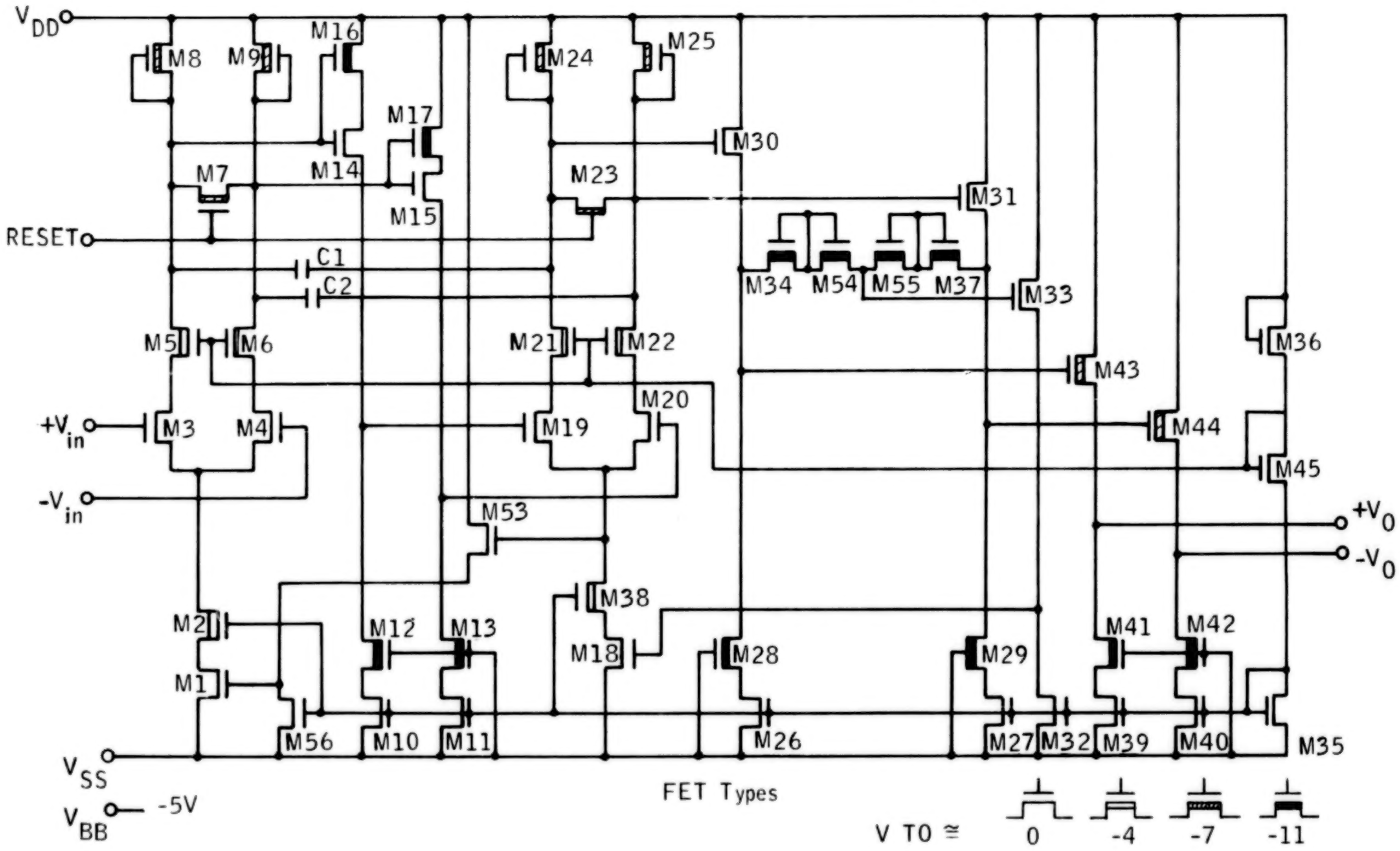
N	$\bar{h}$(cos)	$\bar{h}$(sin)	$\bar{h}$(cos - sin)
512	0.0313	0.0311	1.7×10^{-4}
256	0.0444	0.0439	5.0×10^{-4}
128	0.0632	0.0618	1.4×10^{-3}
64	0.0903	0.0863	4.0×10^{-3}
32	0.130	0.119	1.1×10^{-2}
16	0.189	0.158	3.1×10^{-2}
8	0.274	0.193	8.1×10^{-2}

The difference is small for the larger transforms.

The required equalization of capacitances and cancellation of unwanted signals can then be obtained by substracting the output of a cos and sin chirp filter. In practice, this subtraction is achieved by cross-connecting the V^+ (cos) and V^- (sin) nodes. No additional channel is needed. However, one of the input signals has to be available in both normal and inverted form. Since the length of our transform was small and gain was needed at the inputs to the CCD filters, we chose to use the second approach. Two operational amplifiers are used at the input to the filters and two amplifiers are used as DCIs at the output of the filters. The designs of the two diffamps are identical except for the values of the compensation capacitors and the feedback capacitors.

The basic amplifier is shown in Figure 20 with the design parameters listed in Table I. A photomicrograph of the amplifier is shown in Figure 21.

The amplifier has two stages of differential gain. Each stage is cascaded and uses depletion loads. Between the first and second stages are buffers (M14 and M15) which also serve as level translators. After the second gain stage, the outputs are double-buffered by M30 and M31, and then by M33 and M34. The current source biases of all buffers are cascaded to provide a



V_DD
M8
M9
M16
M24
M25
M17
M30
M14
M7
M23
M31
M15
RESET
C1
C2
M34
M54
M55
M37
M33
M5
M6
M21
M22
M36
M43
M20
+V_in
M3
M4
M19
M44
M45
-V_in
+V_O
-V_O
M53
M38
M2
M12
M13
M41
M42
M18
M28
M29
M1
M56
M10
M11
M26
M27
M32
M39
M40
M35
V_SS
V_BB
-5V
FET Types
V TO ≅
0
-4
-7
-11

Figure 20.- DCI Amplifier Compensated for Gain of 30.

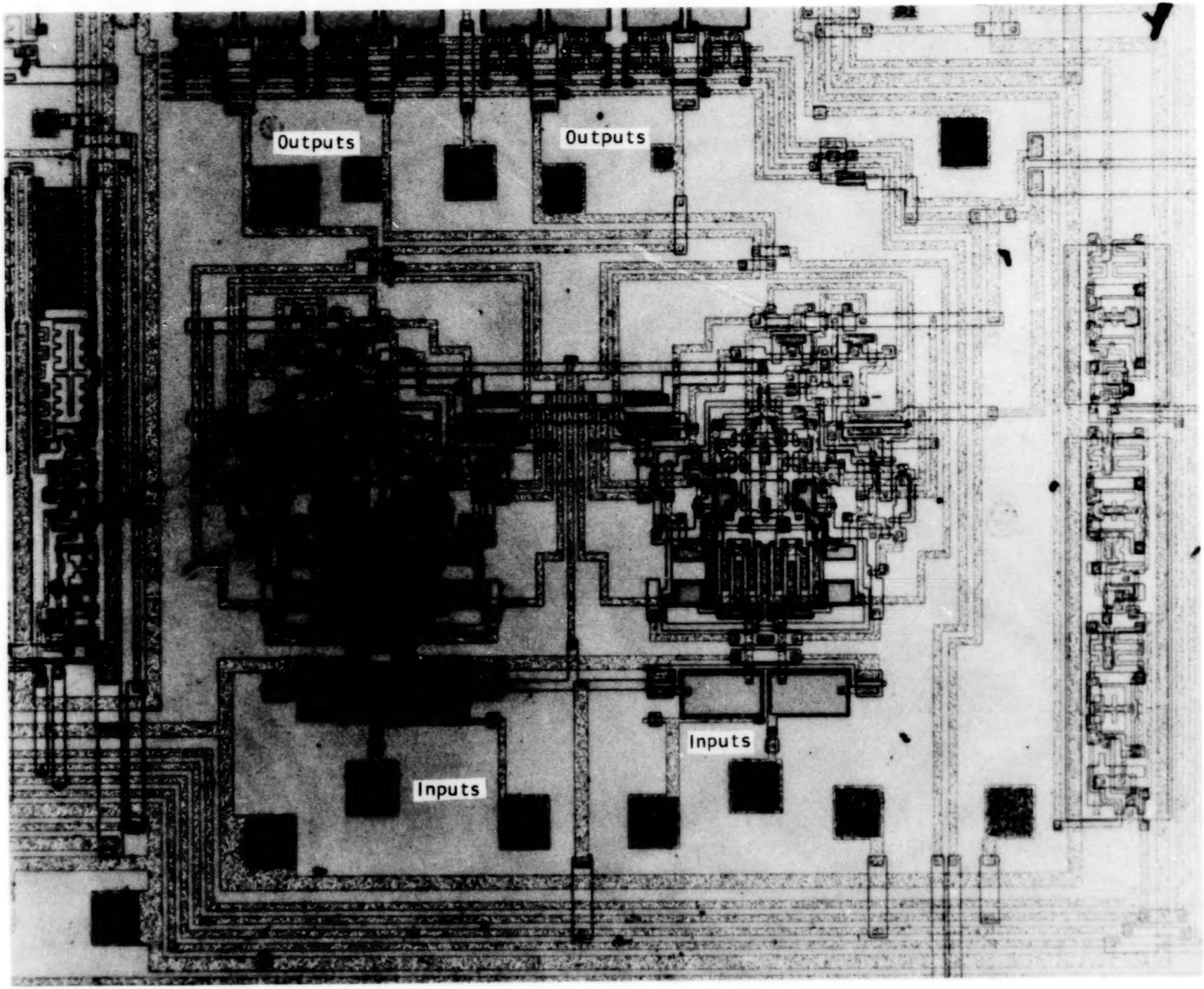

Outputs
Outputs
Inputs
Inputs

Figure 21.- Photomicrograph of Operation Amplifier Used on CZT IC.

Table I

FET Geometries and Supplies

V_{DD} = +20 at 3.5 mA

V_{SS} = 0

V_{BB} = -5 at 1.5 nA

C1 = C2 = 0.075 pF

FETS	W/L (mils)	W/L (μm)
M1, M7, M23	0.35/0.3	8.9/7.6
M2	1.25/0.3	32/7.6
M3, M4	18/0.3	457/7.6
M5, M6	1.30/0.3	33/7.6
M8, M9	0.35/0.7	8.9/17.8
M10,M11	0.7/0.3	17.8/7.6
M12, M13	0.75/0.5	19/12.7
M14, M15	1.5/0.3	38/7.6
M16, M17, M21, M22	0.45/0.5	11.4/12.7
M18	0.6/0.3	15.2/7.6
M19, M20	2.45/0.3	62/7.6
M24, M25	0.35/0.5	8.9/12.7
M26, M27	0.5/0.3	12.7/7.6
M28, M29	0.55/0.5	14/12.7
M30, M31	0.95/0.3	24/7.6
M32	0.7/0.5	17.8/12.7
M33, M41, M42	0.65/0.5	16.5/12.7
M34, M37	0.35/0.65	8.9/16.5
M35	0.75/1.0	19/25.4
M36	0.65/1.7	16.5/43
M38	0.8/0.4	20/10
M39, M40	0.65/0.3	16.5/7.6
M43, M44	5.1/0.3	130/7.6
M45	0.75/1.7	19/43
M53	0.45/0.3	11.4/7.6
M54, M55	0.35/0.85	8.9/22
M56	0.4/0.6	10/15.2

higher output impedance. Dc operating point and common mode rejection are obtained by two overlapping feedback loops connected to the current source of each differential pair.

From the outputs of the second stage to the outputs of the first stage are two compensation capacitors. These capacitors make the second stage look like an integrator, creating a dominant pole in the amplifier's frequency response. This effect is identical to the effect of the compensation capacitor in μA741-type op-amps. The open loop gain of the amplifier is then the gm of the input differential transistors M3 and M4, times the impedance of the compensation capacitors. There is naturally some attenuation through the two output buffers.

$$A = \alpha_{BUF} \frac{g_{m_3}}{SC_{COMP}} ,$$

where

α_{BUF} = attenuation of buffer,

g_{m_3} = forward transfer conductance ratio of MOSFET M3, and

C_{COMP} = value of compensation capacitor.

This formula will hold true for frequencies below the crossover frequency of the inner loop formed by the buffers M14 and M15, the second gain stage, and the feedback path through the compensation capacitors back to the buffers' input. Therefore, the crossover frequency of the op-amp with its integration capacitors must be well below the unity gain point of the inner loop.

The common mode feedback loop dynamics are discussed by stages. In the first stage the gain is the gm of M1 (the first stage current source) times the impedance at nodes 7 and 8 (the first stage outputs) in parallel. The dominant pole is created by the capacitance at those nodes, including the compensation capacitors. The other ends of the compensation capacitors (nodes 18 and 19) tend to be held at virtual grounds by the action of the second stage common node feedback loop.

$$A = \alpha_{BUF} \times g_{m_1} \times 1/SC_2 \quad ,$$

where

α_{BUF} = attenuation of buffer,

g_{m_1} = transconductance of MOSFET M1, and

C_2 = compensation capacitor.

The action of the second stage common mode loop is similar to that of the first stage. Complications arise due to common mode feedback through the compensation capacitors and interactions with the first stage feedback loop. The effect of the first interaction is to create an unwanted pole due to the capacitance at node 15, the sources of the second stage differential pair. Though the second interaction tends to counteract this effect, it is still advisable to minimize the capacitance at node 15 by using the buffer M53 to drive M1.

As in the first stage feedback loop, care must be taken to prevent excessive phase shifting in the buffers which level-translate back down to the current source FETs gate.

The computer-predicted parameters of the two common mode loops are listed on the following page.

	First Stage	Second Stage
Low Frequency Gain	5.5	5.5
Crossover Frequency	14 MHz	22 MHz
Phase Margin	67°	60°

Each amplifier required 47 mW dc power and occupies approximately 0.658 mm^2 (1020 mil^2).

Both the input amplifiers and the DCI amplifiers were modeled using the block diagram of Figure 22. From Figure 22 the closed-loop transfer function is

$$A(s) = \frac{V_o(s)}{V_i(s)} = \frac{a(s)}{1 + a(s)f(s)}$$

where a(s) is the open loop gain,
f(s) is the feedback gain, and
a(s)f(s) is the loop transmission gain.

The stability of each amplifier was based on the loop transmission, a(s)f(s).

A schematic of the input differential amplifier is shown in Figure 23. Transistors Q_1 and Q_2 are used to provide the proper input bias level for the amplifier. Assuming the open loop gain is infinite, the closed loop gain is

$$A(s) = \frac{C_{IN}}{C_{FB}} = \frac{3.0 \text{ pF}}{0.5 \text{ pF}} = 6 \quad ,$$

where C_{IN} is the value of the input capacitance and
C_{FB} is the feedback capacitance.

Both the input capacitors and the feedback capacitors were formed using first and second polysilicon as the capacitor plates. The dielectric constant of the gate oxide between the two polysilicon levels determine the capacitance.

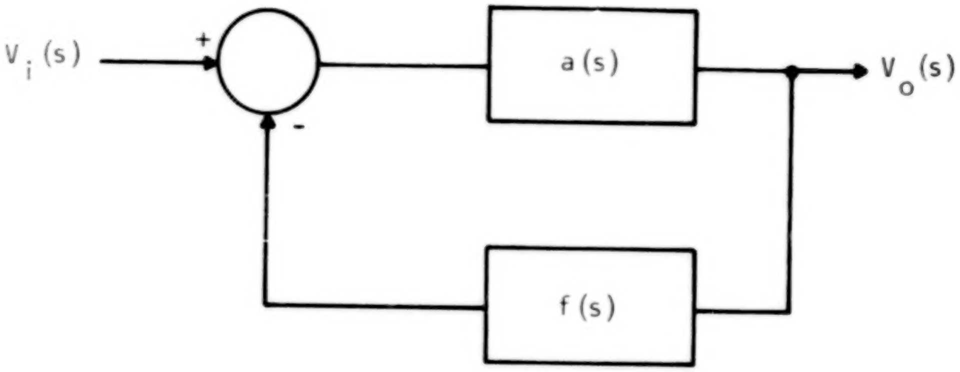

$V_i(s)$
+
-
a(s)
f(s)
$V_o(s)$

Figure 22.- Block Diagram of Single-Loop Amplifier.

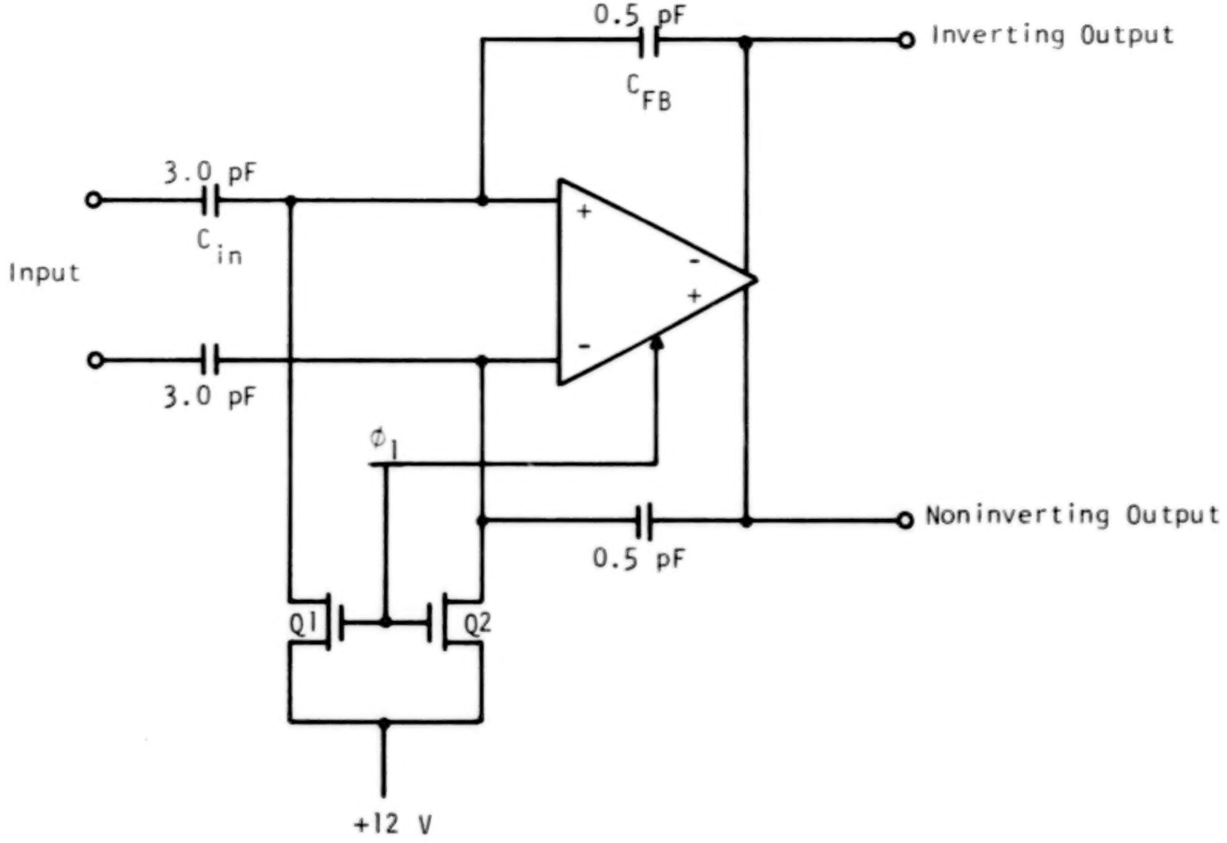

0.5 pF
Inverting Output
C_{FB}
3.0 pF
C_{in}
Input
+
-
-
+
-
3.0 pF
ϕ_1
Noninverting Output
0.5 pF
Q1
Q2
+12 V

Figure 23.-Differential Amplifier.

The amplifier closed loop gain is determined by a capacitance ratio that is also the ratio of the areas of the two polysilicon capacitors. Since these areas can be accurately controlled, the gain is very accurate and predictable. A gain of 6 was chosen to compensate for the attenuation of the MDACs. Based on computer modeling, 1 pF compensation capacitors were chosen.

A plot of the predicted open loop characteristics of the input amplifier is shown in Figure 24. From this plot the following parameters can be obtained:

Crossover Frequency	6 MHz
Feedback Gain	1/6
Gain Bandwidth Product	36 MHz
Phase Margin	63°

The predicted closed loop frequency response is shown in Figure 25. The -3 dB frequency is 9 MHz.

The design of the DCI amplifier is the same as the input amplifier, but instead of providing only signal inversion and gain, the DCI amplifiers function as integrators, integrating the CCD output signal onto the feedback capacitors. A model of the DCI circuit is shown in Figure 26. The CCD output is shown as the split electrodes with a clock driver for each side of the electrodes. Two series-pass MOSFETs (Q_1 and Q_2) are shown that gate the signal into the DCI amplifier. The DCI amplifier uses the ϕ_2' pulse as a reset pulse. The timing of the DCI circuitry is shown in Figure 27.

To prevent the DCI amplifier from seeing a large common mode signal (CCD $\phi_2^{\pm}$), series-pass transistors are used to isolate the amplifier from the split electrodes. To keep the amplifier outputs from drifting apart when the amplifier is isolated, M7 and M23 (Figure 20) were added. When the reset pulse goes high, the outputs of each differential stage are shorted together, holding the outputs of the amplifier at the same bias point. When the reset

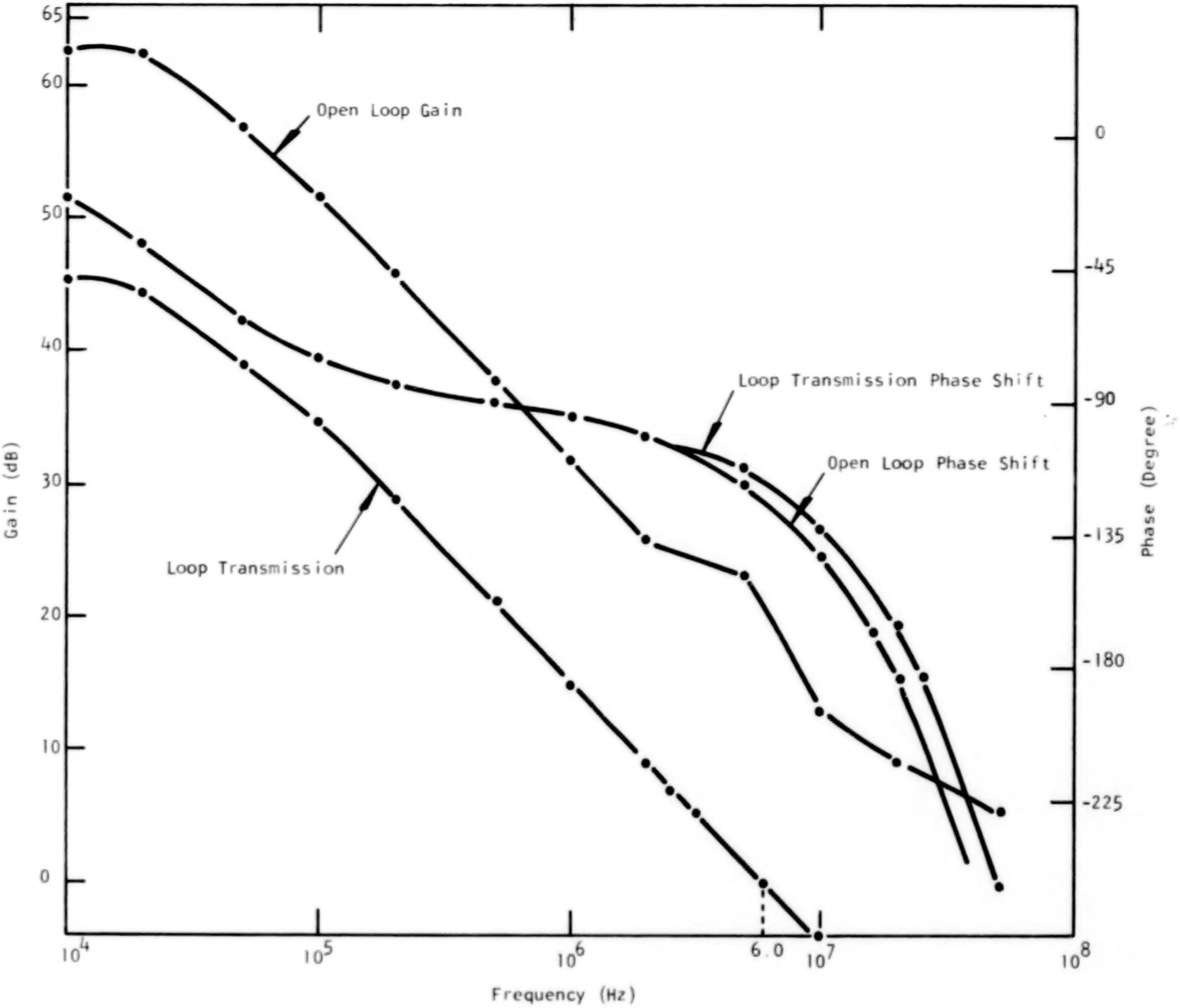


Figure 24.-Differential Amplifier Theoretical Open Loop Characteristics.

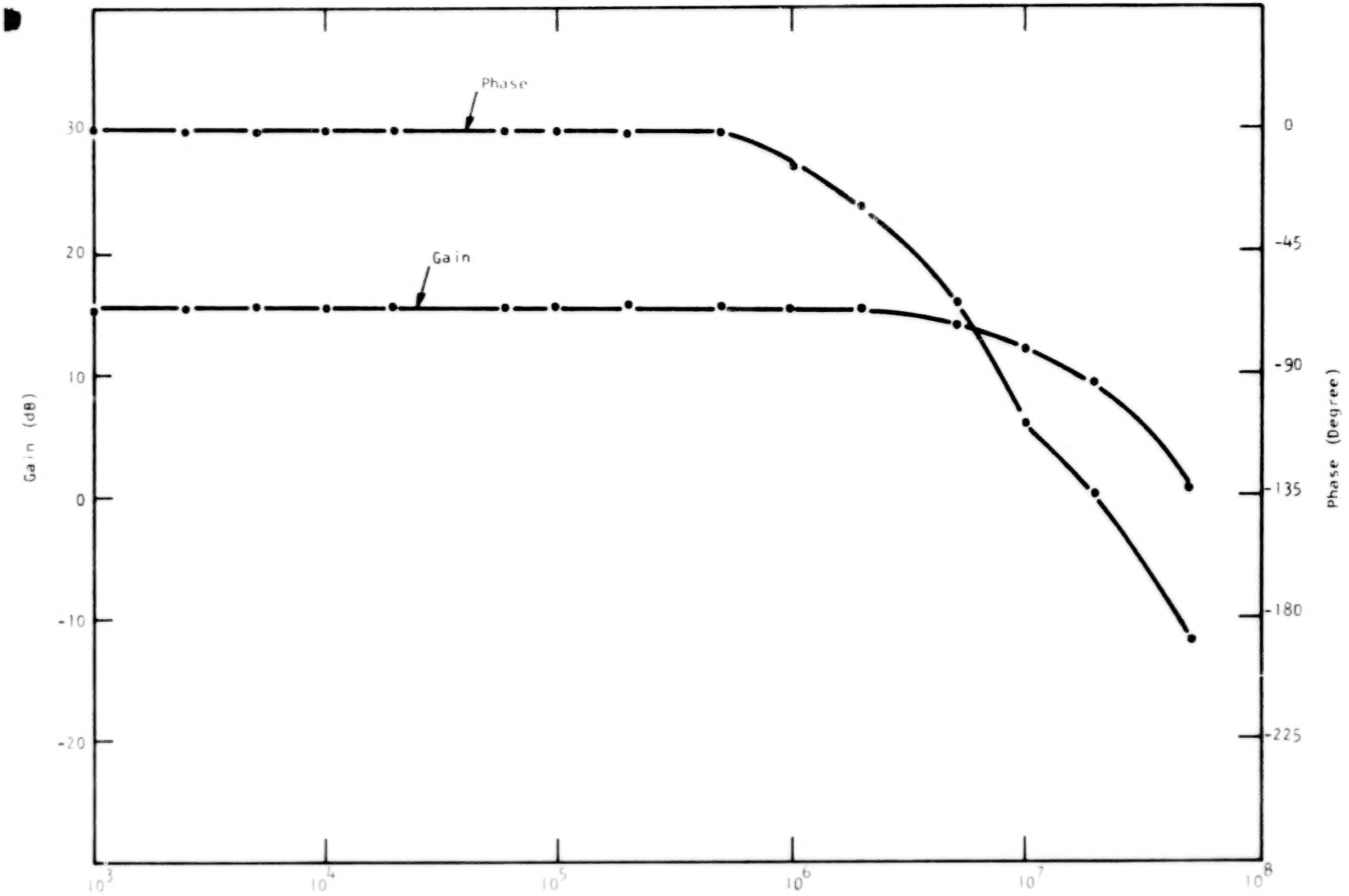


Figure 25.- Input Amplifier Closed Loop Frequency Response.

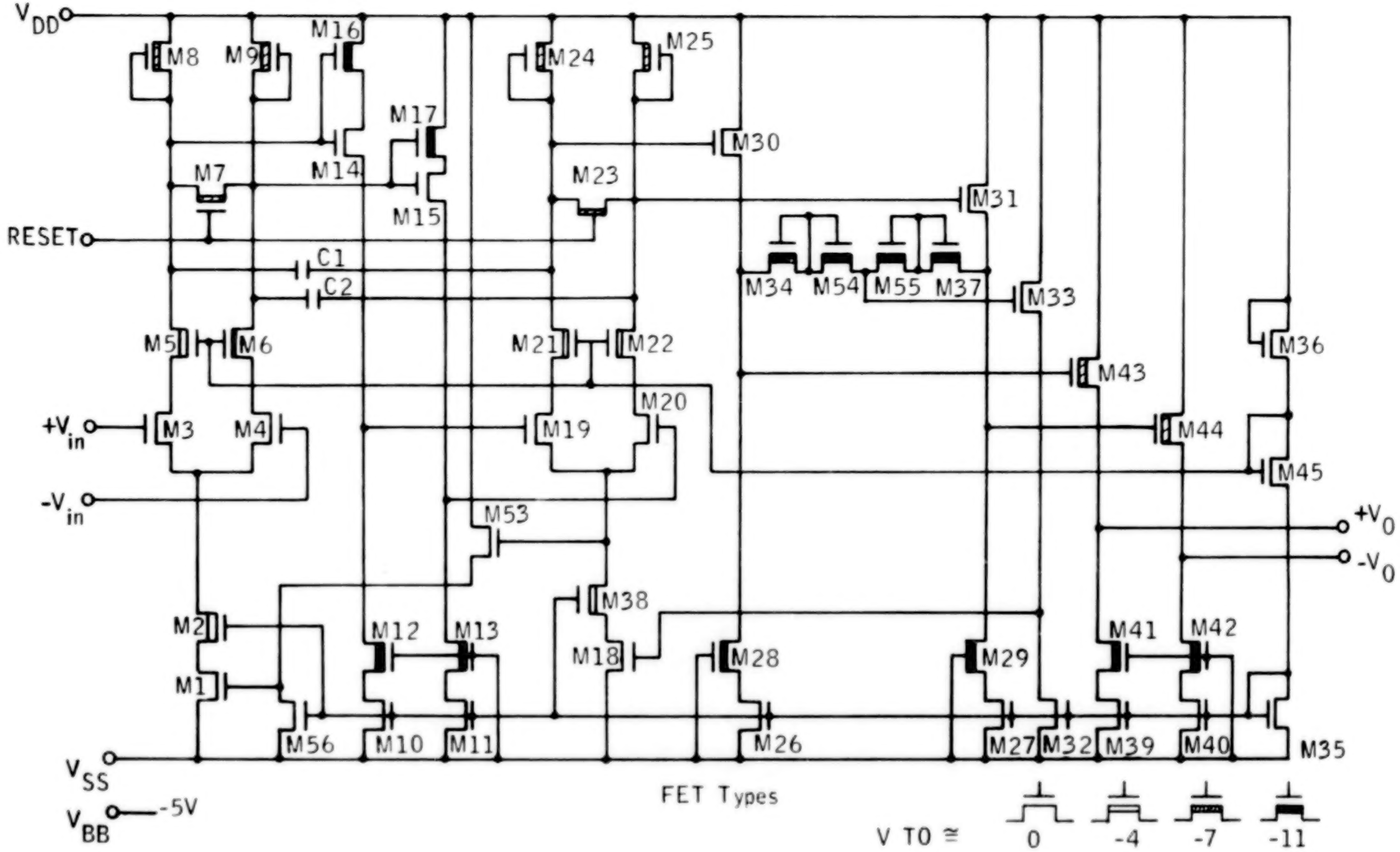

V_DD
M8
M9
M16
M24
M25
M17
M14
M30
M7
M23
M15
M31
RESET
C1
C2
M34
M54
M55
M37
M33
M5
M6
M21
M22
M36
M43
M20
+V_in
M3
M4
M19
M44
M45
-V_in
M53
+V_0
-V_0
M38
M2
M12
M13
M41
M42
M18
M28
M29
M1
M56
M10
M11
M26
M27
M32
M39
M40
M35
V_SS
V_BB
-5V
FET Types
V TO ≅
0
-4
-7
-11

Figure 26.- DCI Amplifier.

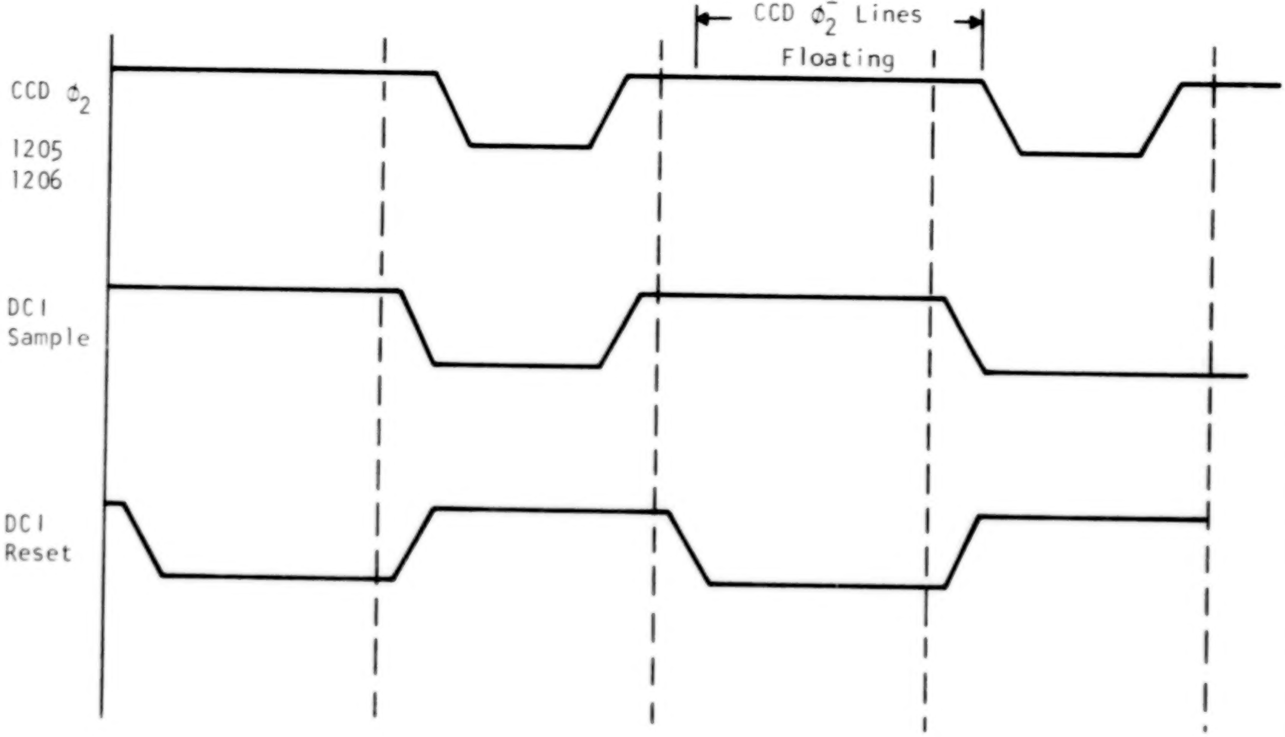

CCD $\phi_2^{\pm}$ Lines Floating
CCD ϕ_2
1205
1206
DCI Sample
DCI Reset

Figure 27.- DCI Timing.

pulse is off and the DCI sample pulse is high, the amplifier outputs settle to a new bias point and the signal output of the amplifier is the difference between this new bias point and voltage swing of the amplifier.

While the CCD $\phi_2^{\pm}$ clock lines are held low, the DCI amplifier is reset with the DCI reset pulse (ϕ_2'). Also, the DCI sample pulse is off, isolating the $\phi_2^{\pm}$ electrodes from the DCI amplifier. Before the $\phi_2^{\pm}$ electrodes are allowed to float, the DCI sample pulse goes high, connecting the amplifier to the split electrodes. Next, the reset pulse goes low, and the amplifier is ready to integrate the signal charge onto its feedback capacitors when the CCD ϕ_1 clock goes low. A photograph showing the CCD clocks is shown in Figure 28. The time the CCD $\phi_2^{\pm}$ clock is floating is indicated by the arrows.

The gain from the CCD filter input to the DCI amplifier output can be calculated from the input charge of the CCD filter

$$Q_{in} = C_{in} V_{in} \quad ,$$

where C_{in} is the input well capacity and
V_{in} is the input voltage,
and the output charge

$$Q_{out} = N(\tfrac{1}{2})\ C_{in} V_{in} \quad ,$$

where N is the number of points in the transform (32).
The factor of $\frac{1}{2}$ arises when a non-dc input is assumed. Since

$$Q_{out} = C_{out}\ V_{out}$$

then

$$V_{out} = \frac{Q_{out}}{C_{out}} = \frac{16\ C_{in} V_{in}}{C_{out}} \quad ,$$

where C_{out} is the feedback capacitor of the DCI amplifier.

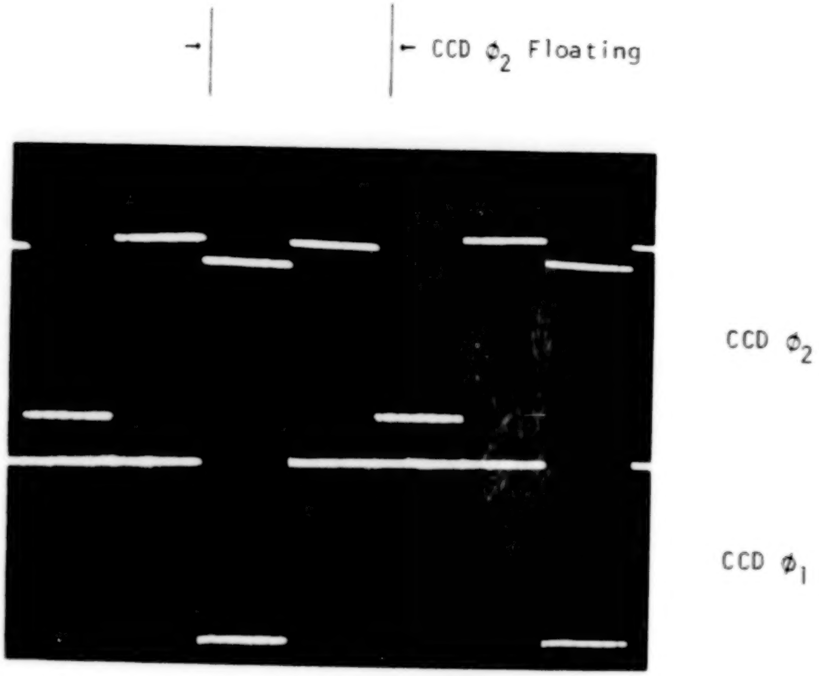


Figure 28.-CCD Clocks.

Solving for C_{out}:

$$C_{out} = \frac{16\ C_{in} V_{in}}{V_{out}} = 16 \times 0.26 \times \left(\frac{V_{in}}{V_{out}}\right) = 4.16\ \text{pF}\left(\frac{V_{in}}{V_{out}}\right) \quad .$$

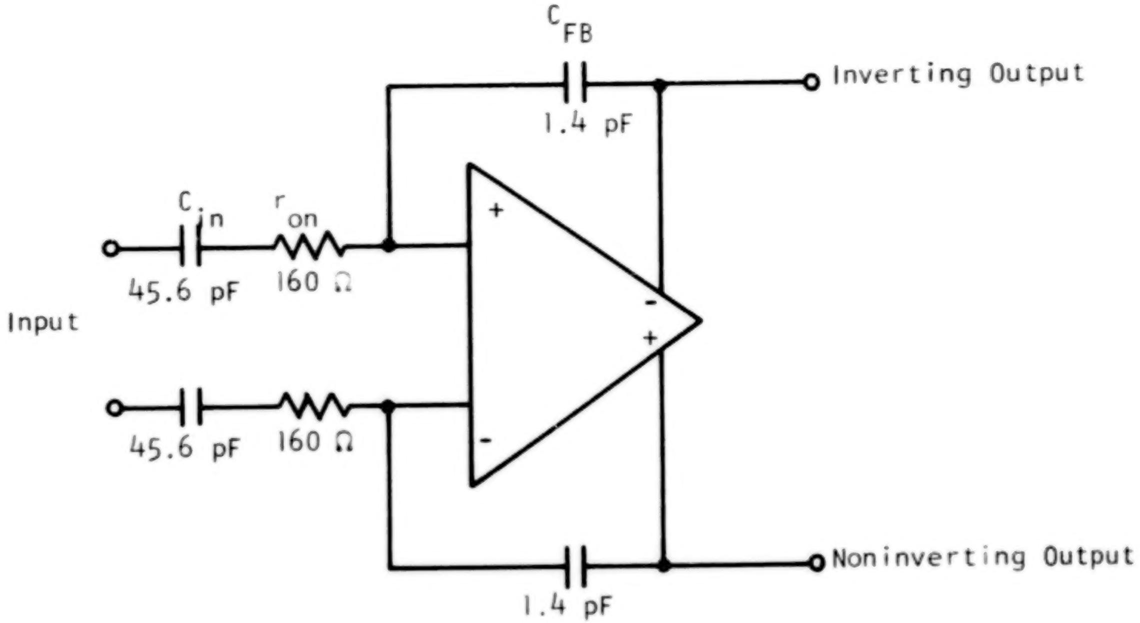
To provide some gain to overcome the attenuation of the following ac-couple/dc-restore circuitry and the output source-follower, a value of 1.4 pF was chosen for the feedback capacitor. Substituting this value into the gain equation yields

$$\text{Gain} = \frac{V_{out}}{V_{in}} = \frac{16\ C_{in}}{C_{out}} = \frac{16 \times 0.26\ \text{pF}}{1.4\ \text{pF}} = 3 \quad .$$

A model for computer simulation of the DCI amplifier only is shown in Figure 29. This model was constructed to examine the characteristics of the amplifier. The CCD split electrode has been modeled as an equivalent capacitor, and the on-resistance of the series-pass transistors has been calculated to be 160 Ω, based on the physical size of the MOSFETs and the gate-to-source voltage. A model for calculating the CCD $\phi_2^{\pm}$ capacitance is shown in Figure 30. The values of the capacitors for two filters in parallel are:

Depletion capacitance	$C_{dep} = 4.6$ pF
Oxide capacitance	$C_{OX} = 41.4$ pF
First poly-to-moat and metal-to-substrate	$C_1 = 5.38$ pF
Overlap of CCD ϕ_1	$C_2 = 19.2$ pF
Overlap to $\overline{\text{CCD}\phi_1}$	$C_3 = 19.2$ pF .

These capacitances can be combined into one equivalent capacitor for gain calculations.



C FB
1.4 pF
Inverting Output
C in
r on
45.6 pF
160 Ω
Input
45.6 pF
160 Ω
+
-
-
+
1.4 pF
Noninverting Output

Figure 29.-Model for DCI.

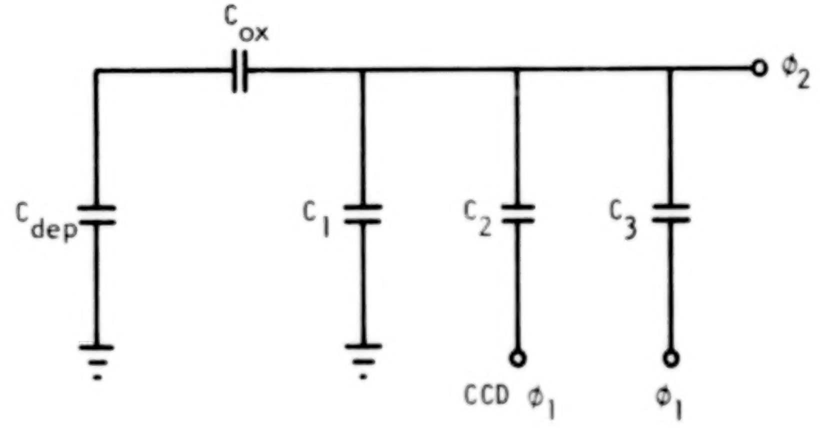

C_ox
ϕ_2
C_dep
C_1
C_2
C_3
CCD ϕ_1
ϕ_1

Figure 30.-Capacitance Model for DCI Input.

The predicted open loop characteristics of the DCI amplifier are shown in Figure 31. From this figure the following parameters can be calculated:

Crossover frequency	17 MHz
Feedback gain	1/32
Gain-bandwidth product	550 MHz
Phase margin	65°.

The predicted closed loop frequency response of the DCI amplifiers is shown in Figure 32, and the -3 dB frequency is seen to be 25 MHz.

2. Experimental Results

Experimental results have been obtained for the input amplifiers using the test setup shown in Figure 33. A pulse generator was used as the inputs to the amplifiers, and attenuators were used to obtain low-level signals. Because there are two input amplifiers, the inverting inputs and the noninverting inputs were connected to allow testing of both amplifiers. The input signal and the inputs of the amplifiers were connected through the connection box in a number of ways, depending on the test performed. Because the output signal of the amplifiers has a large dc component, an ac-couple/dc-restore circuit was used. Finally, the output signal was sampled so that a digital voltmeter could be used to record the test results. As can be seen in Figure 33, both the input signals and all the output signals were recorded through the same ac-couple/dc-restore and sample-and-hold circuit.

The results of the amplifier tests are shown in Figures 34 - 36. Figure 34 shows the single-ended transfer characteristics of the amplifier. The single-ended gain is approximately 3, and output is linear up to about 0.4 V input. Figure 35 is a plot of the response of the amplifier to a common mode input signal. The differential mode characteristics are shown in Figure 36.

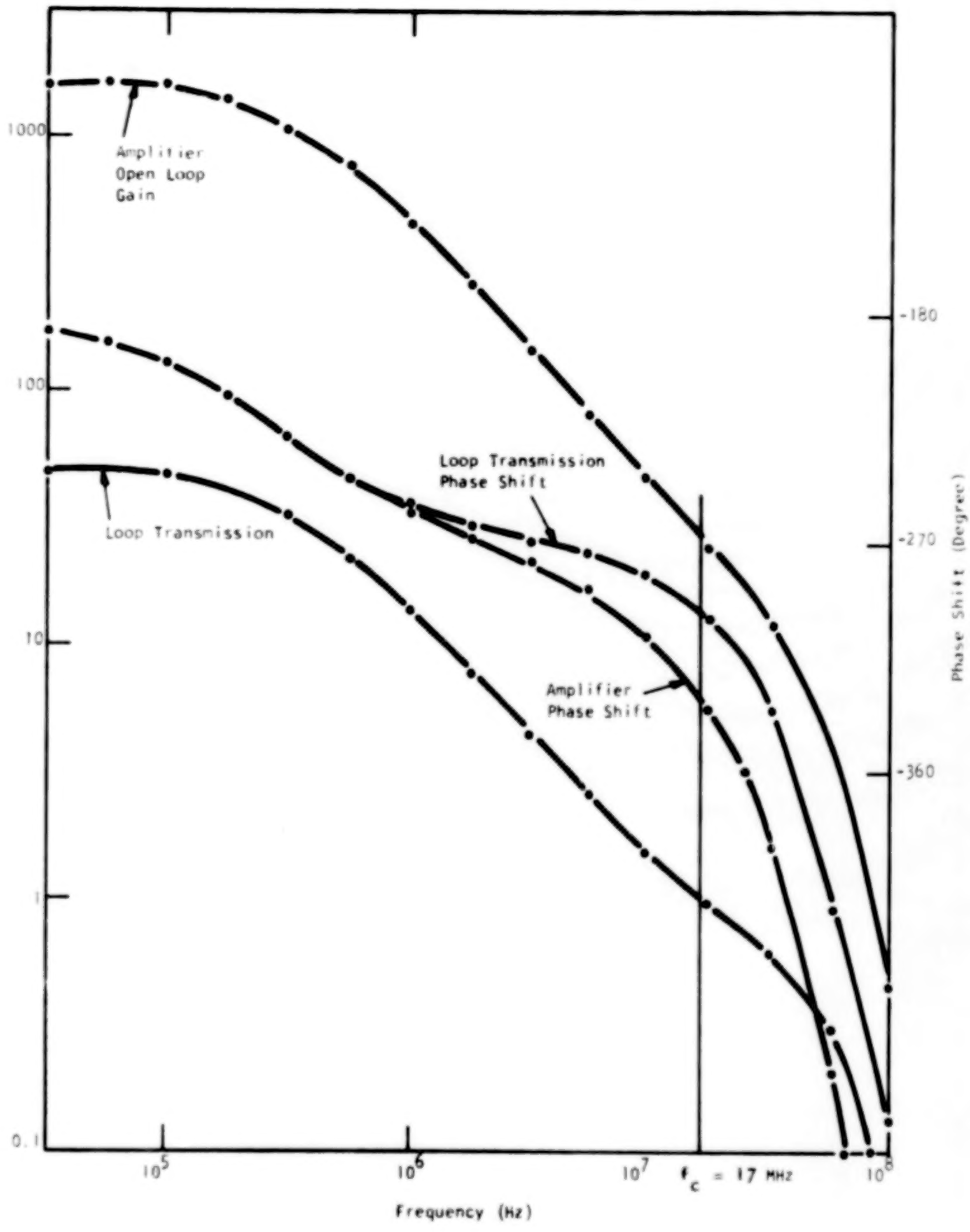


Figure 31. - DCI Diff-Amp Open Loop Performance.

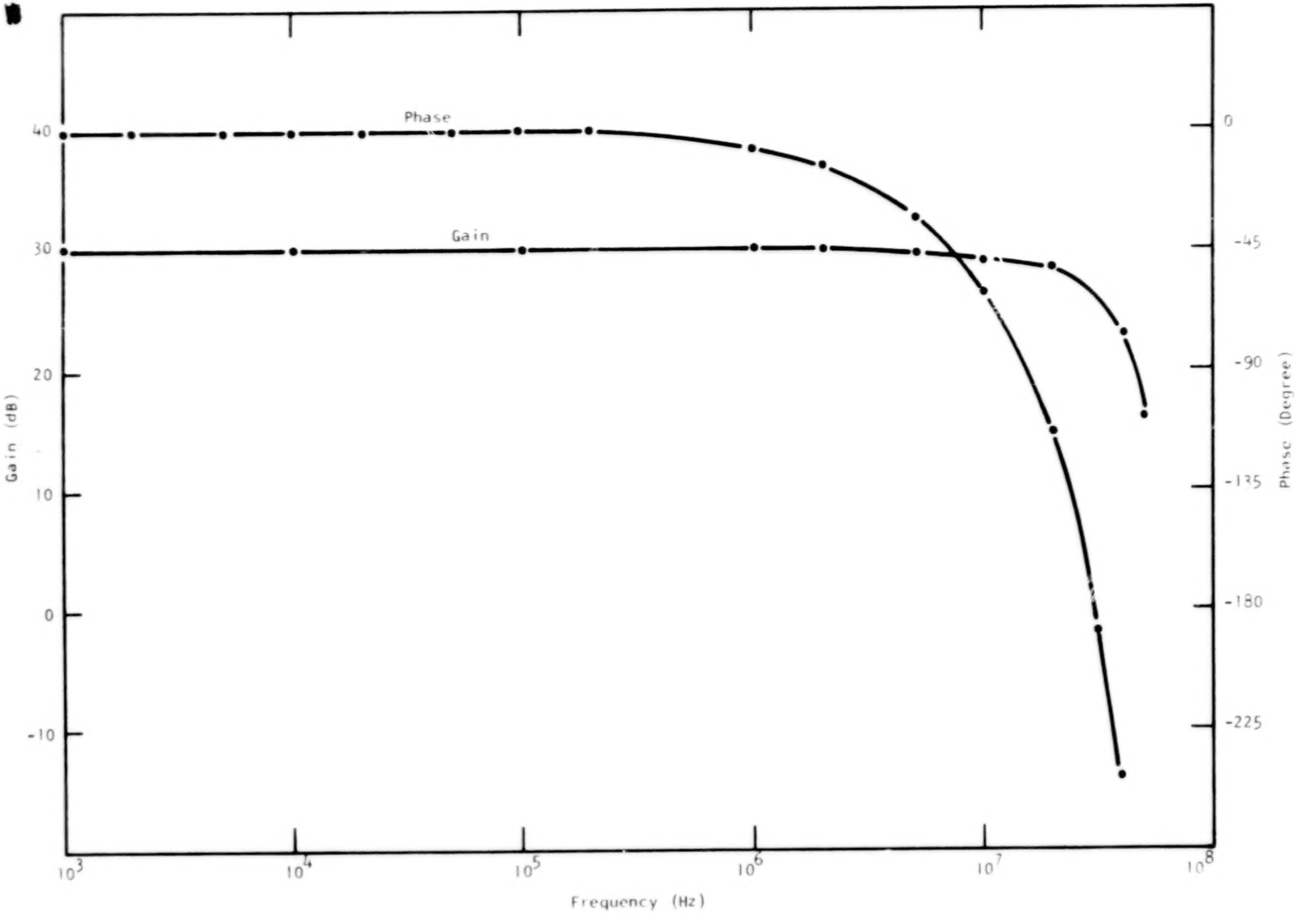


Figure 32.- Closed Loop Frequency Response of DCI Amplifier.

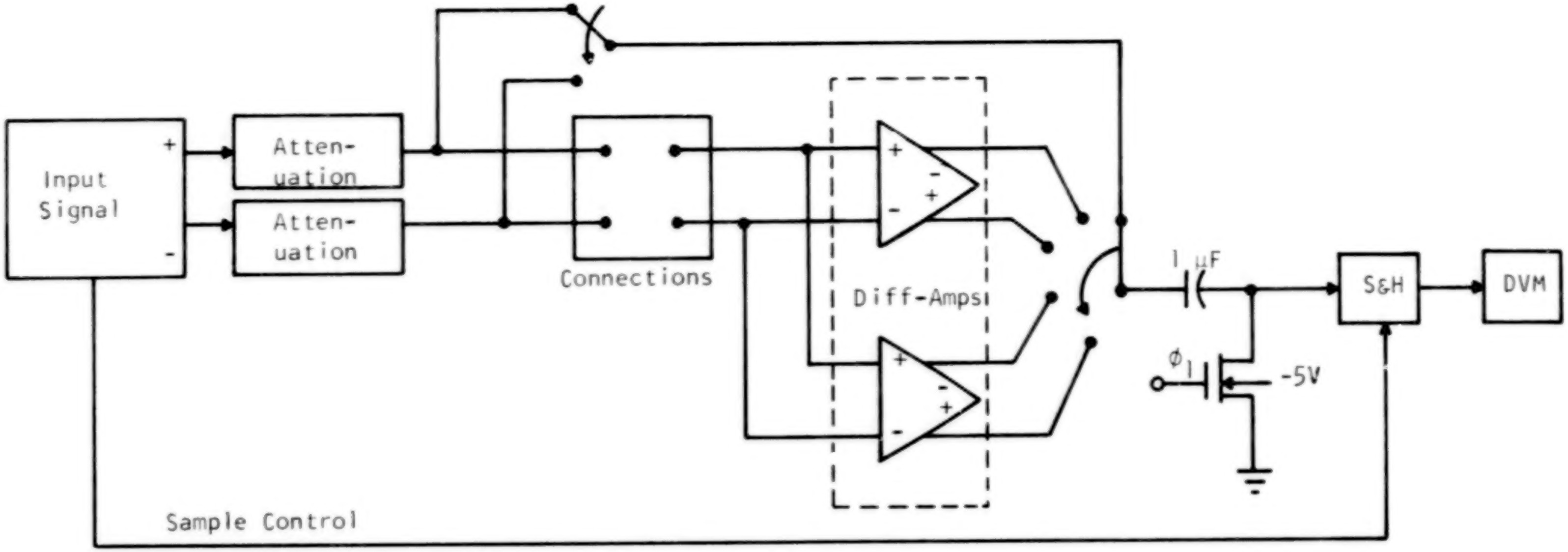

Input
Signal
+
-
Atten-
uation
Atten-
uation
Connections
Diff-Amps
+
-
-
+
+
-
-
+
1 μF
ϕ_1
-5V
S&H
DVM
Sample Control

Figure 33.- Differential Amplifiers Test.

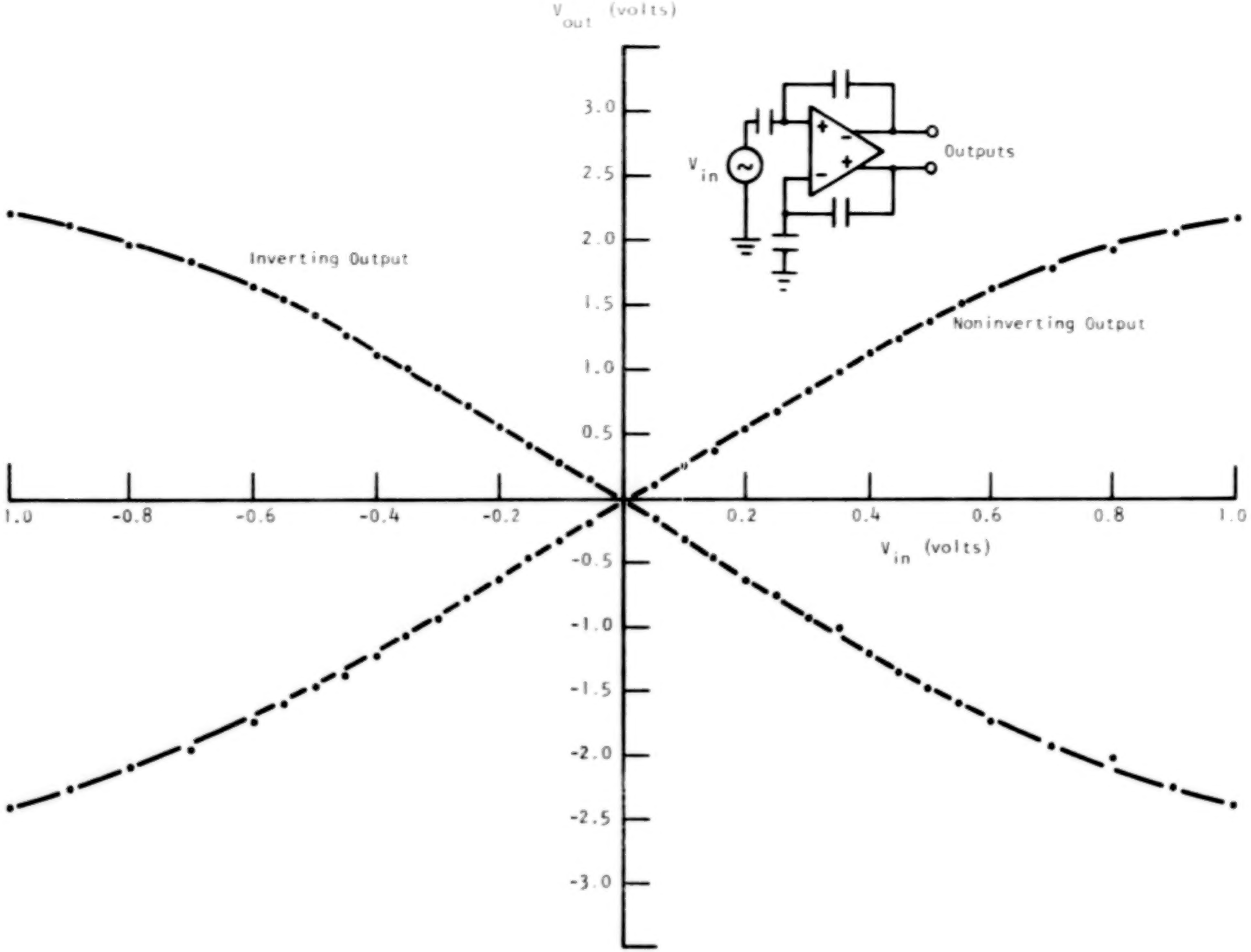


Figure 34.-Single-Ended Transfer Characteristics of Input Differential Amplifier.

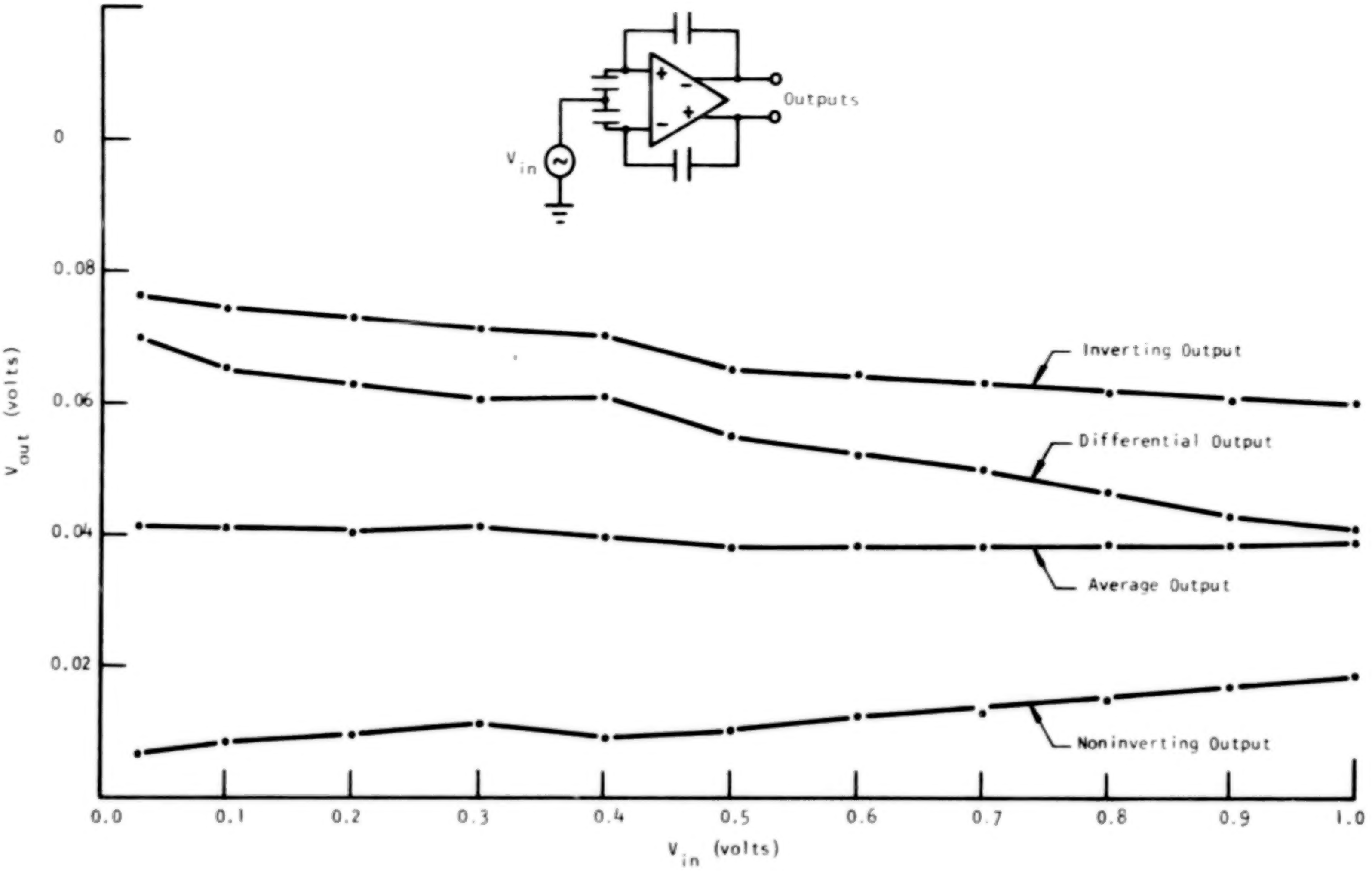


Figure 35.- Response of Input Differential Amplifier to Common Mode Input.

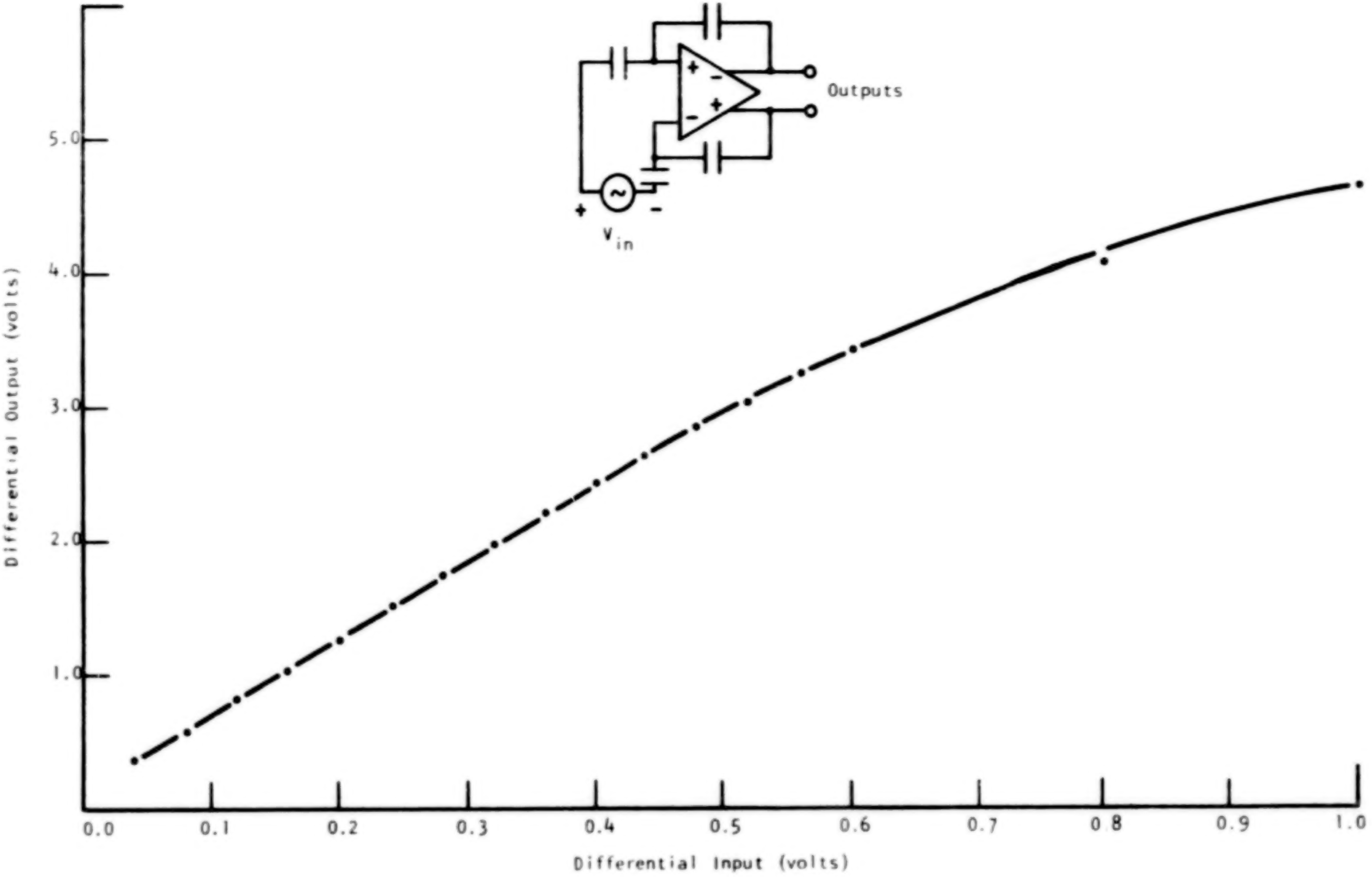


Figure 36.-Differential Mode Characteristics of Input Amplifier.

Some photographs of the input amplifier in operation are shown in Figures 37 and 38. Figure 37 shows the single-ended output of the amplifier with a ramp input. Figure 38 shows two photographs of the input amplifier. In the top photograph the input and output signals of the amplifier are shown, and again the gain can be measured to be approximately 3. The bottom photograph is better for determining gain and linearity. The horizontal axis has been calibrated so that it corresponds to the differential input voltage. The vertical axis is the single-ended output of the amplifier. By comparing the amplifier output to the ideal straight-line output which has been superimposed, one can see the output becomes very nonlinear above 0.6 V input. The open-loop transient characteristics of the DCI amplifier are shown in Figure 39. The top photograph shows the open-loop dc transfer curve, and the bottom photograph shows the open-loop step response. The rise time is about 1.6 μs.

D. Multiplying Digital-to-Analog Converters (MDACs)

Four multiplying D/A converters (MDACs) are on the CZT IC. These perform the pre- and post-multipliers of the CZT algorithm. They also perform multiplication by the reference for the correlation and filtering configurations. Each MDAC output is an analog signal whose value is proportional to the product of an analog input signal and a digital word. For the CZT pre- and post-multiplications, the required chirp signals are stored digitally on chip in a ROM. For multiplication by a reference, the digital signal must be supplied externally.

1. Design

Each MDAC consists of an input sample-and-hold circuit, ROM sense and MDAC drive circuitry, a capacitor array and an output buffer. A photograph of two MDACs is shown in Figure 40.

The MDAC minus the sample-and-hold and ROM sense/MDAC circuitry is shown in Figure 41 with W/L and capacitor values indicated. This circuit

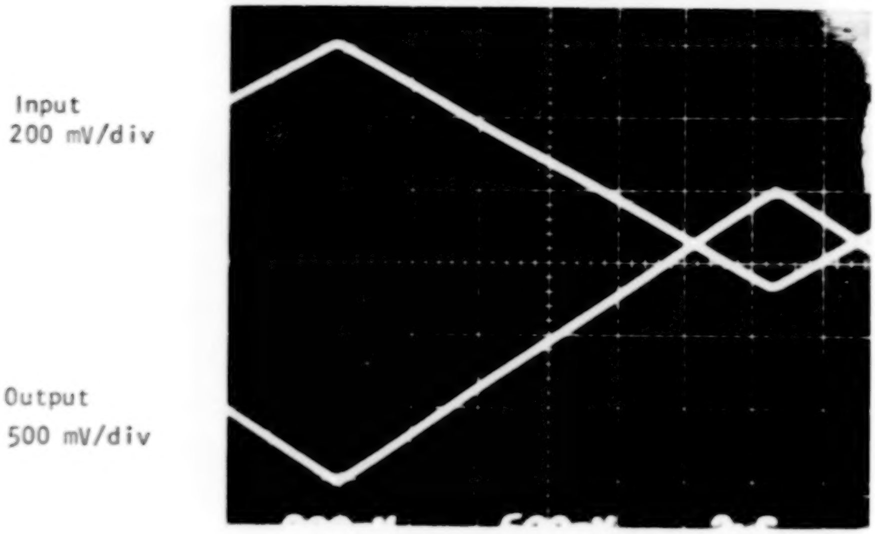
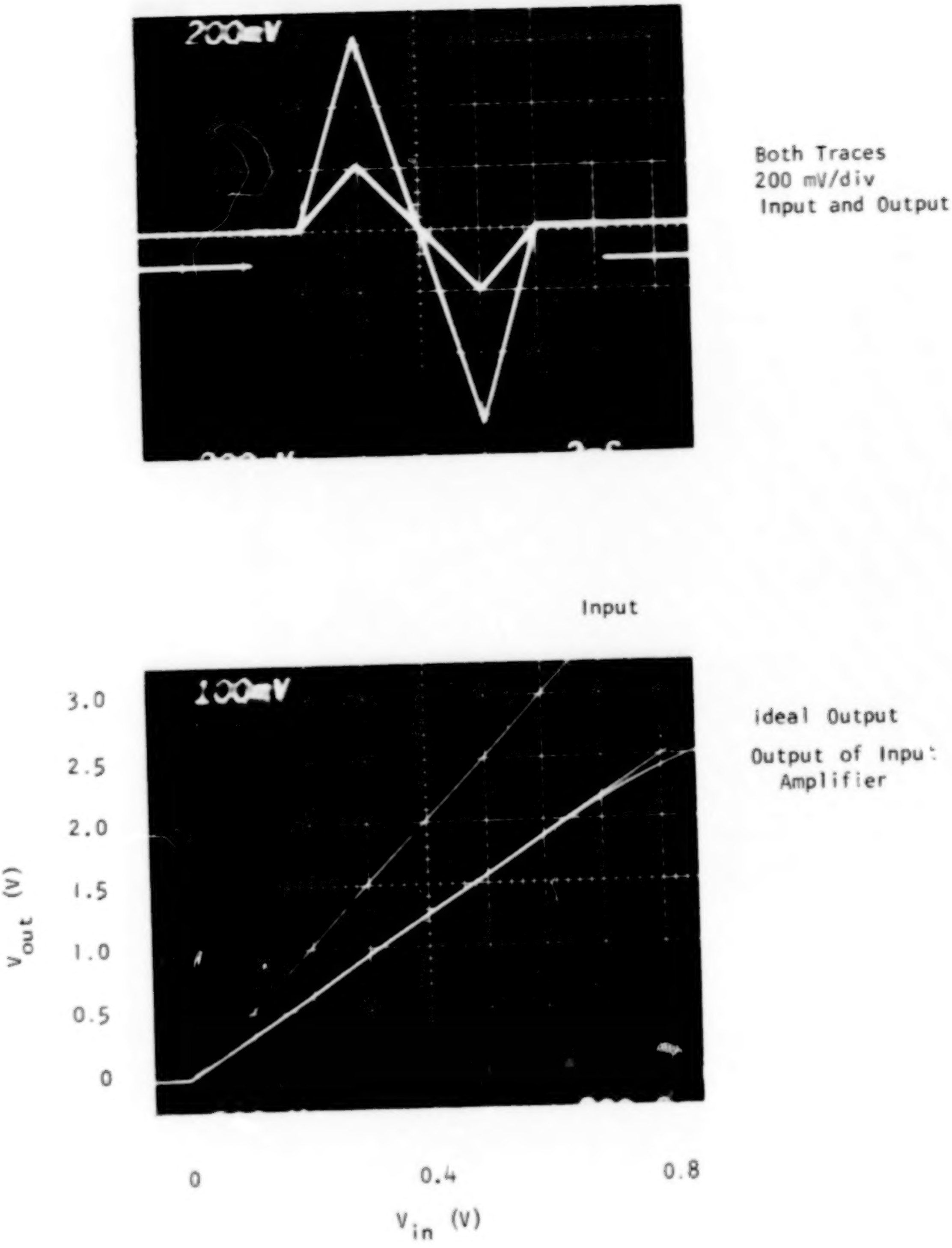


Figure 37.- Single-Ended Response of Differential Amplifier to Ramp Input.



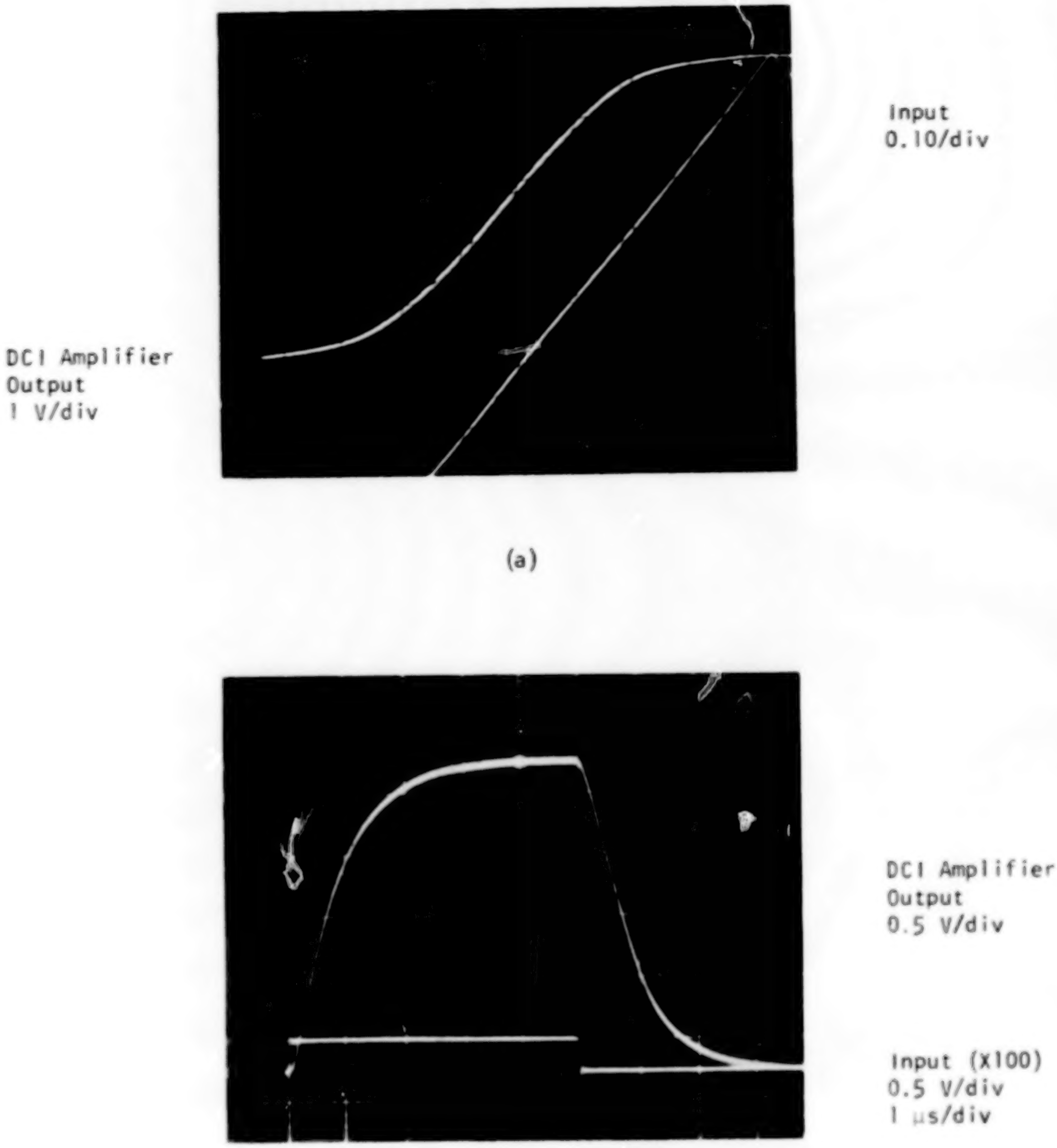
Both Traces
200 mV/div
Input and Output

Input

Ideal Output

Output of Input
Amplifier

Figure 38.-Photograph Showing the Gain and Linearity of Input Amplifiers.



(a)

(b)

Figure 39.-DCI Amplifier Open Loop Characteristics.

TABLE OF CONTENTS

SECTION		PAGE	
I	INTRODUCTION	1	1/A12
	A. Frequency Domain Correlation	3	1/B1
	B. Time Domain Correlation	8	1/B6
II	32-POINT CCD CZT IC	14	1/B14
	A. Chip Overview	14	1/B14
	B. CCD Filter	22	1/C13
	C. Operational Amplifiers	27	1/D6
	1. Design	27	1/D6
	2. Experimental Results	52	1/F12
	D. Multiplying Digital-to-Analog Converters (MDACs)	59	1/G11
	1. Design	59	1/G11
	2. Experimental Results	71	2/A14
	E. Read-Only Memory (ROM) and ROM Address	71	2/A14
	1. Read-Only Memory	71	2/A14
	2. Up/Down Ring Counter (ROM Address)	82	2/C3
	3. Synchronization	87	2/C9
	F. Timing Circuitry	98	2/D10
	1. Clock Generators	98	2/D10
	2. Experimental Results	109	2/E10
	G. Experimental Results	114	2/F3
	H. Applications	121	2/F11
III	64-POINT CCD ANALOG/ANALOG CORRELATOR	125	2/G5
	A. Design	125	2/G5
	B. Performance Limitations in Design	129	2/G12
	1. Multiplier Nonlinearity	129	2/G12
	2. Offsets	132	3/A4
	3. Input Stage Offsets and Nonlinearities	133	3/A5
	C. Measured Performance	133	3/A5
	1. CCD Signal Capacity	133	3/A5
	2. Feedback Linearized Input Stage	134	3/A6

TABLE OF CONTENTS

(Continued)

SECTION PAGE

3. Multiplier Linearity. 136 3/A8
4. Offsets 140 3/A13
5. Multiplier Scale Factor Matching. 148 3/B7
6. Evaluation. 148 3/B7

D. Directions for Future Designs. 150 3/B9
1. System Organization 150 3/B9
2. CCD Design. 152 3/B11
3. Input Stage Design. 152 3/B11
4. Buffer Design 152 3/B11
5. Multipliers 153 3/B12

E. Applications and Summary 153 3/B12
1. Applications. 153 3/B12
2. Summary 153 3/B12

IV CCD BINARY/ANALOG CORRELATOR. 155 3/B14
A. Introduction 155 3/B14
B. Binary/Analog Programmable CCD Correlator Technology 159 3/C4
C. Application of Binary/Analog Correlator to Pattern Classification 171 3/D7
D. Preliminary Design of Matrix Multiplier IC 174 3/D10
E. Four-Sensor Demonstration Unit 177 3/D13

V CONCLUSIONS 182 3/E4

REFERENCES. 184 3/E6

LIST OF ILLUSTRATIONS

FIGURE PAGE

1 Block Diagram of a Transversal Filter Showing Delay Stages D and Weighting Coefficients h_n n = 0, N - 1. 2
2 Schematic of the CZT Algorithm. 5
3 Interpretation of the CZT in Terms of Chirp Input Waveforms in Chirp Filters. 6
4 Block Diagram of a CCD Programmable Correlator. 7
5 Block Diagram of the Analog/Analog Time Domain Correlator 9
6 Circuit Schematic of the Four-Quadrant Multiplier Used in the Analog/Analog Correlator of Figure 5. 10

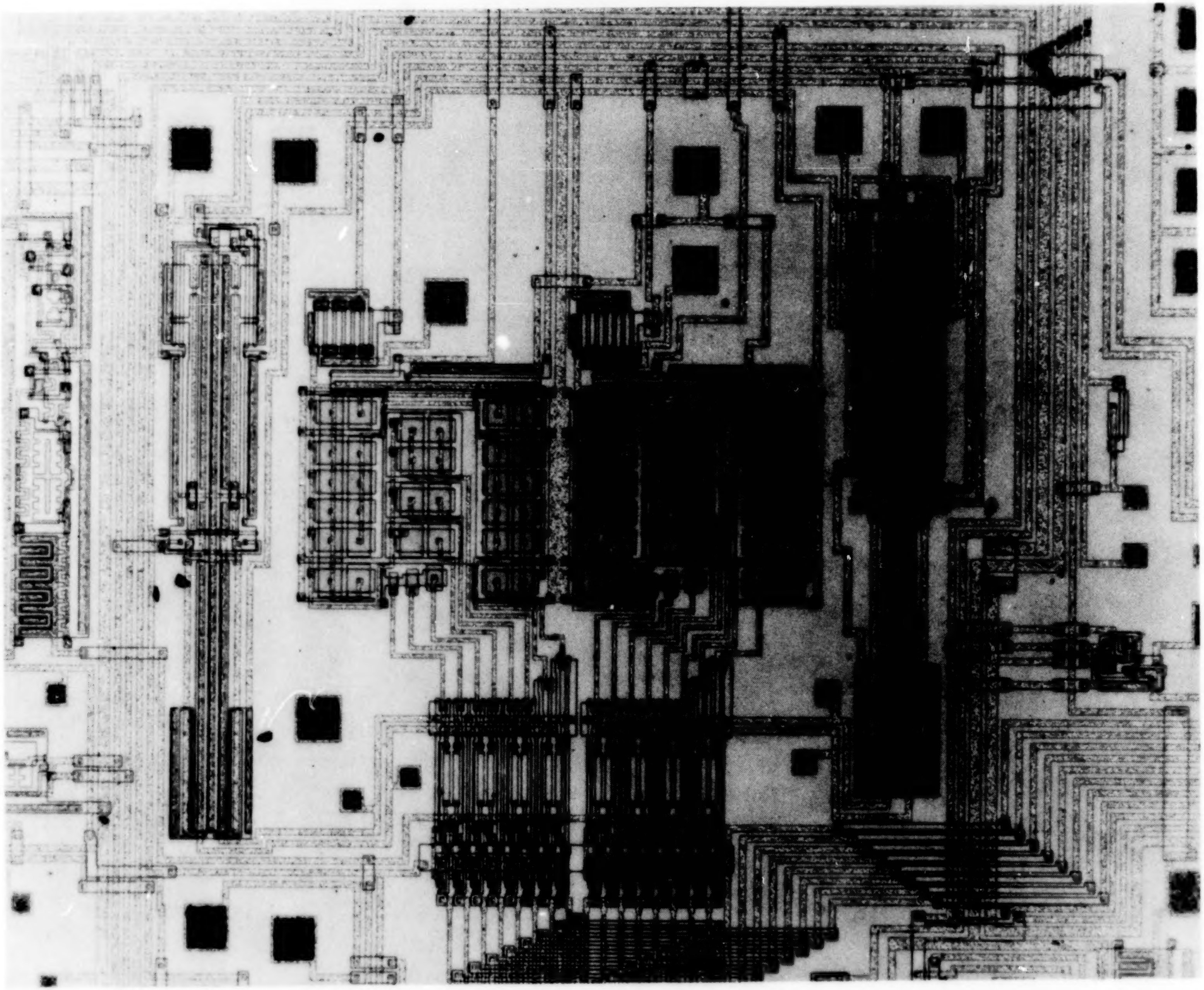
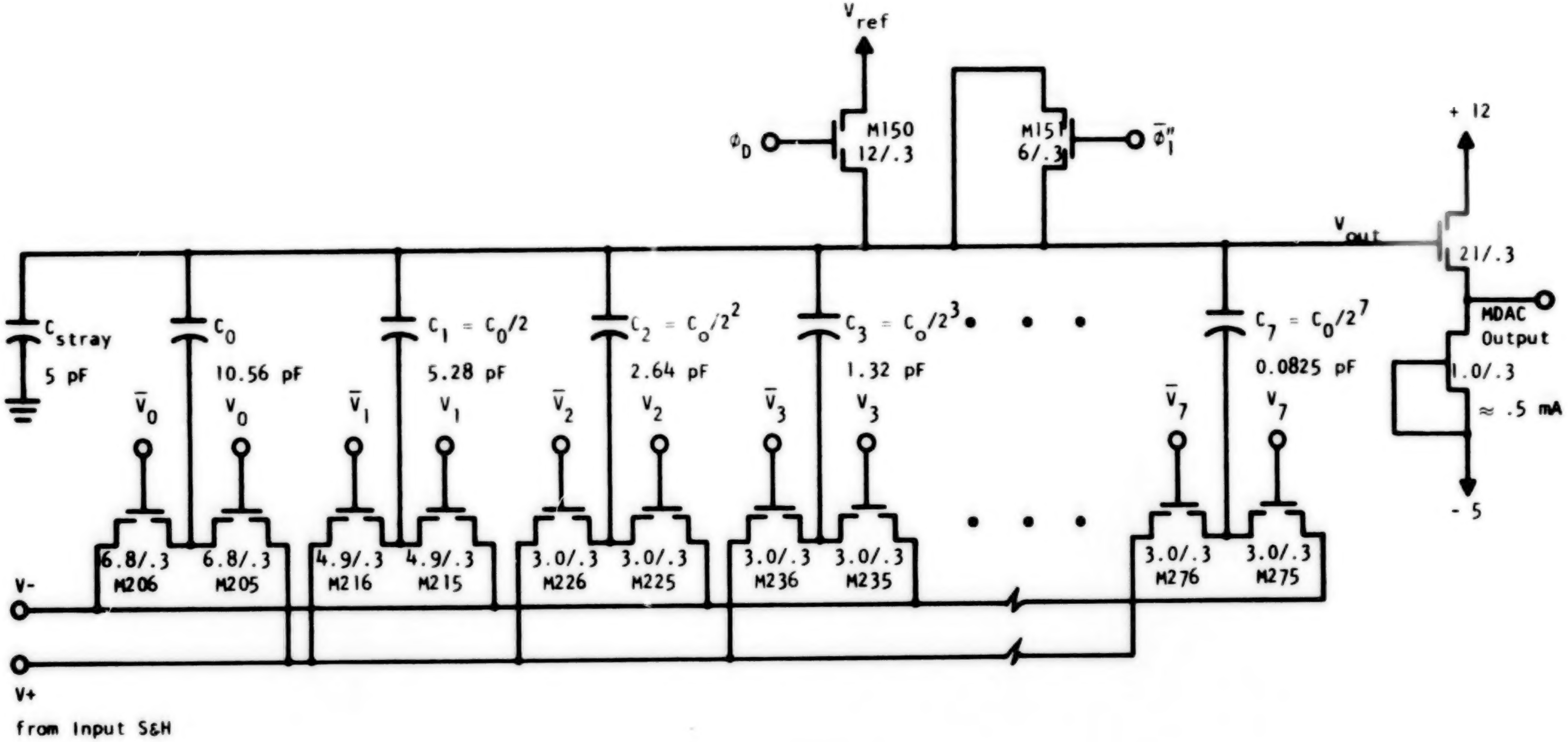


Figure 40.-Photograph of Dual MDACs Used on CZT IC.



V_{ref}
ϕ_D
M150
12/.3
M151
6/.3
$\bar{\phi}_1''$
+ 12
V_{out}
21/.3
MDAC Output
1.0/.3
≈ .5 mA
- 5
C_{stray}
5 pF
C_0
10.56 pF
$C_1 = C_0/2$
5.28 pF
$C_2 = C_o/2^2$
2.64 pF
$C_3 = C_o/2^3$
1.32 pF
$C_7 = C_0/2^7$
0.0825 pF
$\bar{V}_0$
V_0
$\bar{V}_1$
V_1
$\bar{V}_2$
V_2
$\bar{V}_3$
V_3
$\bar{V}_7$
V_7
6.8/.3
M206
6.8/.3
M205
4.9/.3
M216
4.9/.3
M215
3.0/.3
M226
3.0/.3
M225
3.0/.3
M236
3.0/.3
M235
3.0/.3
M276
3.0/.3
M275
V-
V+
from Input S&H

Figure 41.- MDAC.

performs a full four-quadrant multiplication using a capacitor divider network. For noninverting operation, a sampled input signal is applied to the V^+ line, and a reference voltage is applied to the V^- line. During the initial portion of each clock cycle, the common output node (V_{out}) of the capacitor array is clamped to V_{ref} through M150 by ϕ_D (refer to Figure 44). Also, the switching signals v_i are high, and $\overline{v}_i$ are low. (The v_i and $\overline{v}_i$ waveforms are nonoverlapping complementary waveforms.) This connects the largest capacitor to the signal V^+ and all other capacitors to the reference V^- through the switching transistors M205 through M275. Next, ϕ_D goes low, leaving the common node floating. A complementary pulse to ϕ_D ($\overline{\phi}_1''$) is capacitively coupled to the common node by M151 to reduce the level translation of V_{out} when M150 is turned off. Next, the $\overline{v}_i$ and v_i signals corresponding to "1"s at the i^{th} bits, b_i, of the digital word are inverted, causing capacitors C_i to be switched from one input line to the other through the M2i6s. The $\overline{v}_i$ and v_i corresponding to B_i = "0" remain unchanged. The result of switching capacitor C_i from one input line to the other is that the common node voltage, V_{out}, is changed by an amount $\pm (V_+ - V_-)[(C_o/2^i \times b_i)/(2C_o + C_{stray})]$. This change has a positive sign for $i = 1$ to 7 and a negative sign for $i = 0$, since b_o is the sign bit. The resulting output, V_{out}, for multiplication by an arbitrary digital word is given by superposition to be

$$V_{out} = V_{ref} + (V_+ - V_-)\left(\frac{C_o}{2C_o + C_{stray}}\right) \times [-b_o + \sum_{i=1}^{n} b_i \, 2^{-i}] \quad .$$

Two's complement coding is used for the digital word.

The output voltage V_{out} of the MDAC is equal to the product of the signal voltage $(V_+ - V_-)$ and the digital input word times the attenuation factor $C_o/(2C_o + C_{stray})$. For $C_{stray} = 0$, the maximum possible gain is ½. The actual stray capacitance was calculated to be 5 pF, making the gain to the common node $V_{out} = 10.56/(2 \times 10.56 + 5) = 0.4$. The capacitor array was formed by using first polysilicon to second polysilicon capacitance. First polysilicon was used as the output node, and the major source of the stray capacitance is from the first polysilicon to the substrate. To control the capacitance ratios in the capacitor divider network, the larger capacitors were formed as binary multiples of a smaller capacitor. Capacitor C_4 is a 51 μm x 51 μm (2 mil x 2 mil) poly-poly capacitor with a value of about 0.66 pF. Capacitor C_3 is obtained by tying two 51 μm x 51 μm poly-poly capacitors together so that $C_3 = 2C_4 = 1.32$ pF. The three larger capacitors are formed by tying 51 μm x 51 μm capacitors together ($C_2 = 4C_4$, $C_1 = 8C_4$, $C_0 = 16C4$). In this way, the correct capacitor ratios are obtained without maintaining perfect control of the absolute capacitance. The capacitors C_5, C_6, and C_7 are formed by smaller poly-poly areas, since a small error in their value will not significantly affect the output accuracy. An attempt was made in layout to keep all 51 μm x 51 μm capacitors identical by placing dummy first poly around certain parts of the array to maintain identical first poly edges. The V^+ and V^- inputs required for the MDAC are supplied by the buffered sample-and-hold circuit shown in Figure 42. The V^+ and V^- outputs are from identical stages so that the circuit can be used in either an inverting or a noninverting mode. For noninverting operation, the signal voltage is applied to the + input, and a reference voltage corresponding to the dc value of the signal voltage is applied to the - input. The signal is buffered by the first souce-follower (M101, M102, M103) and is sampled by the input sample-and-hold pulse through M104. The holding capacitor consists of a 2 pF first polysilicon to second polysilicon capacitor and the gate capacitance of M107 for a total of about 5.3 pF. The sampled signal is buffered by a second source-follower (M105, M106, M107) before being applied to the MDAC. This second source-follower was designed to drive the capacitive load of the MDAC at clock frequencies of up to 2.5 MHz. This accounts for the large device size of M107. $\overline{\phi}_1$ is a pulse approximately complementary to the input sample-and-hold pulse. It is applied to the gated capacitor M114 to reduce the nonlinear level translation occurring when M104 is turned off. Dual series current sources are used in the source-

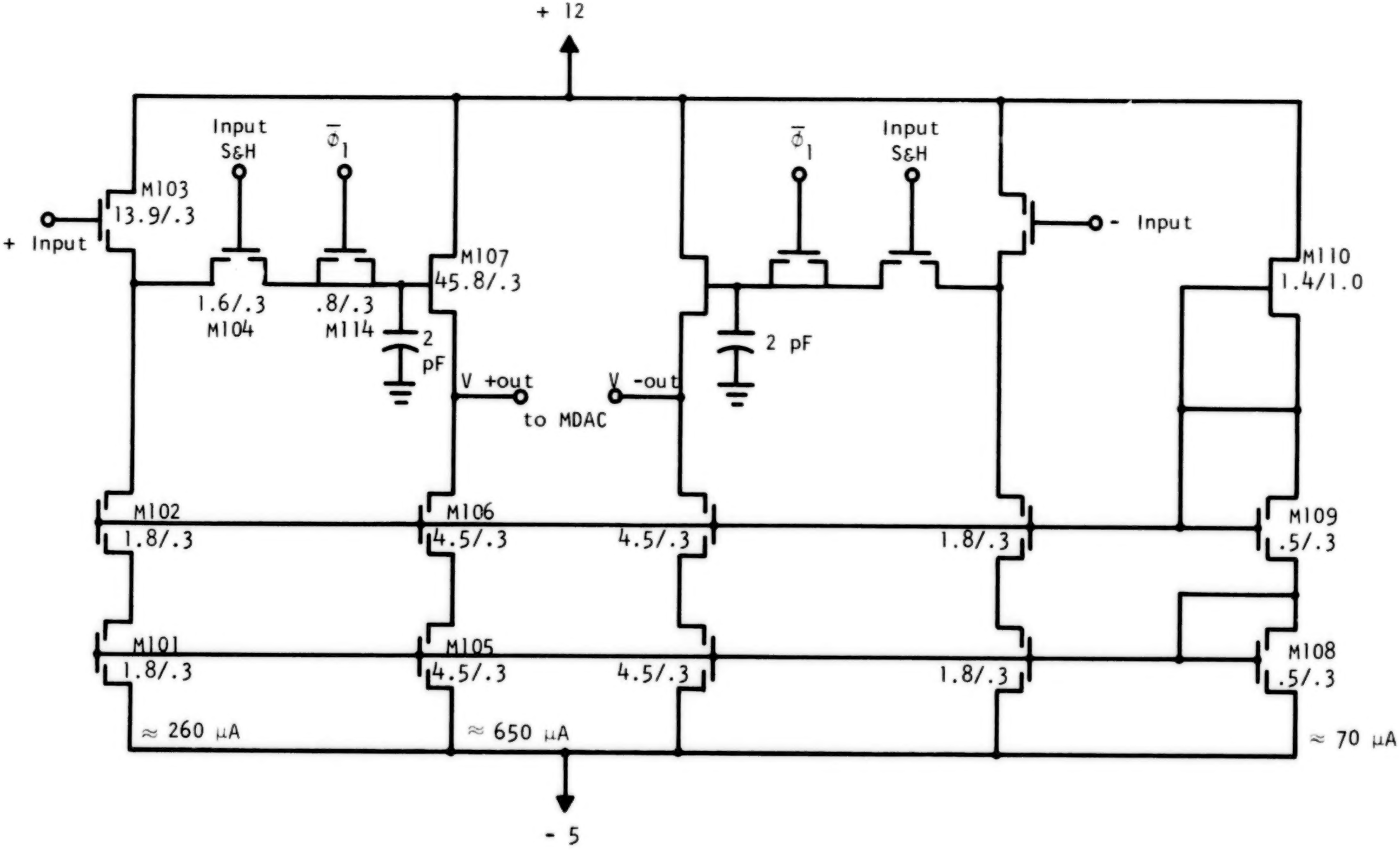

+ 12
Input S&H
$\overline{\phi}_1$
M103
13.9/.3
+ Input
1.6/.3
M104
.8/.3
M114
2 pF
M107
45.8/.3
V +out
V -out
to MDAC
2 pF
$\overline{\phi}_1$
Input S&H
- Input
M110
1.4/1.0
M102
1.8/.3
M106
4.5/.3
4.5/.3
1.8/.3
M109
.5/.3
M101
1.8/.3
M105
4.5/.3
4.5/.3
1.8/.3
M108
.5/.3
≈ 260 μA
≈ 650 μA
≈ 70 μA
- 5

Figure 42.- Buffered Input Sample-and-Hold.

followers to decrease the effect of λ (the channel length modulation parameter) on the gain. The gates of the current sources are fed by the voltage division stage consisting of M108, M109, and M110. The gain of each source-follower is 0.9, making the gain of the entire buffered sample-and-hold circuit 0.81.

The switching signals $\bar{v}_i$ and v_i are supplied by the ROM sense and MDAC drive circuitry shown in Figure 43. Each MDAC contains eight of these circuits. ϕ_B and ϕ_C are complementary nonoverlapping clocks. ϕ_B comes up during the first portion of each clock cycle, pulling v_i up (if it is not already up), and charging the gates of M201 and M204 to the value of the ROM (or external word) output voltage. This voltage will be high if b_i = "1" and low if b_i = "0". If b_i = "1", the gate of M201 will be high and v_i will fall with ϕ_B. Then ϕ_C comes up, pulling $\bar{v}_i$ up since the gate of M204 is high. M114 is a gated capacitor that bootstraps the gate voltage of M204 high enough to allow $\bar{v}_i$ to reach the full voltage of ϕ_C. At the end of the clock cycle, $\bar{v}_i$ falls with ϕ_C. If b_i = "0", the gate of M201 will be low, and v_i remains high when ϕ_B falls. Since the gate of M204 is uncharged, $\bar{v}_i$ does not come up with ϕ_C.

The switching waveforms and typical signal waveforms for a multiplication by 0.5 are illustrated in Figure 44. The digital word is 01000000. The v_1 and $\bar{v}_1$ pulses switch the bottom plate of capacitor C_1 from the V^- line to the V^+ line (Figure 41) to accomplish the multiplication by 0.5. The MDAC output is valid while ϕ_C is up after the signal has settled.

The only dc power consumed by the entire MDAC is in the four source-followers and the voltage divider of the buffered sample-and-hold stage and in the output buffer of the MDAC. The total dc power consumed by these stages in one MDAC is 40 mW.

The total attenuation of the signal from the buffered input to the buffered output is 0.3. This is the result of transmission through three source-followers with gains of 0.9 each, and the MDAC capacitor array with a gain of 0.4.

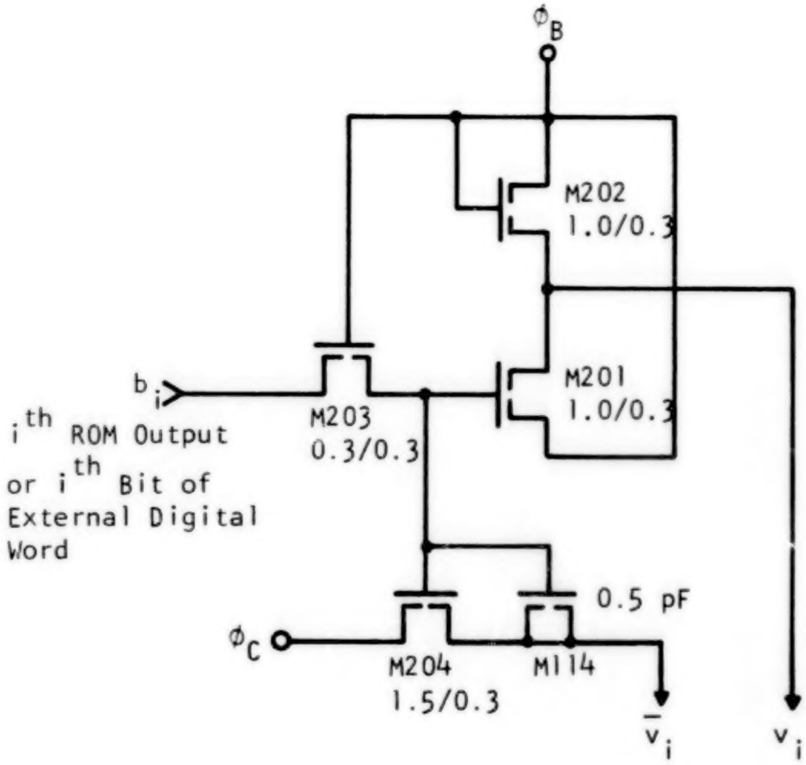

ϕ_B
M202
1.0/0.3
M201
1.0/0.3
b_i
i^{th} ROM Output
or i^{th} Bit of
External Digital
Word
M203
0.3/0.3
0.5 pF
ϕ_C
M204
1.5/0.3
M114
$\bar{v}_i$
v_i

Figure 43.- ROM Sense and MDAC Drive Circuitry.

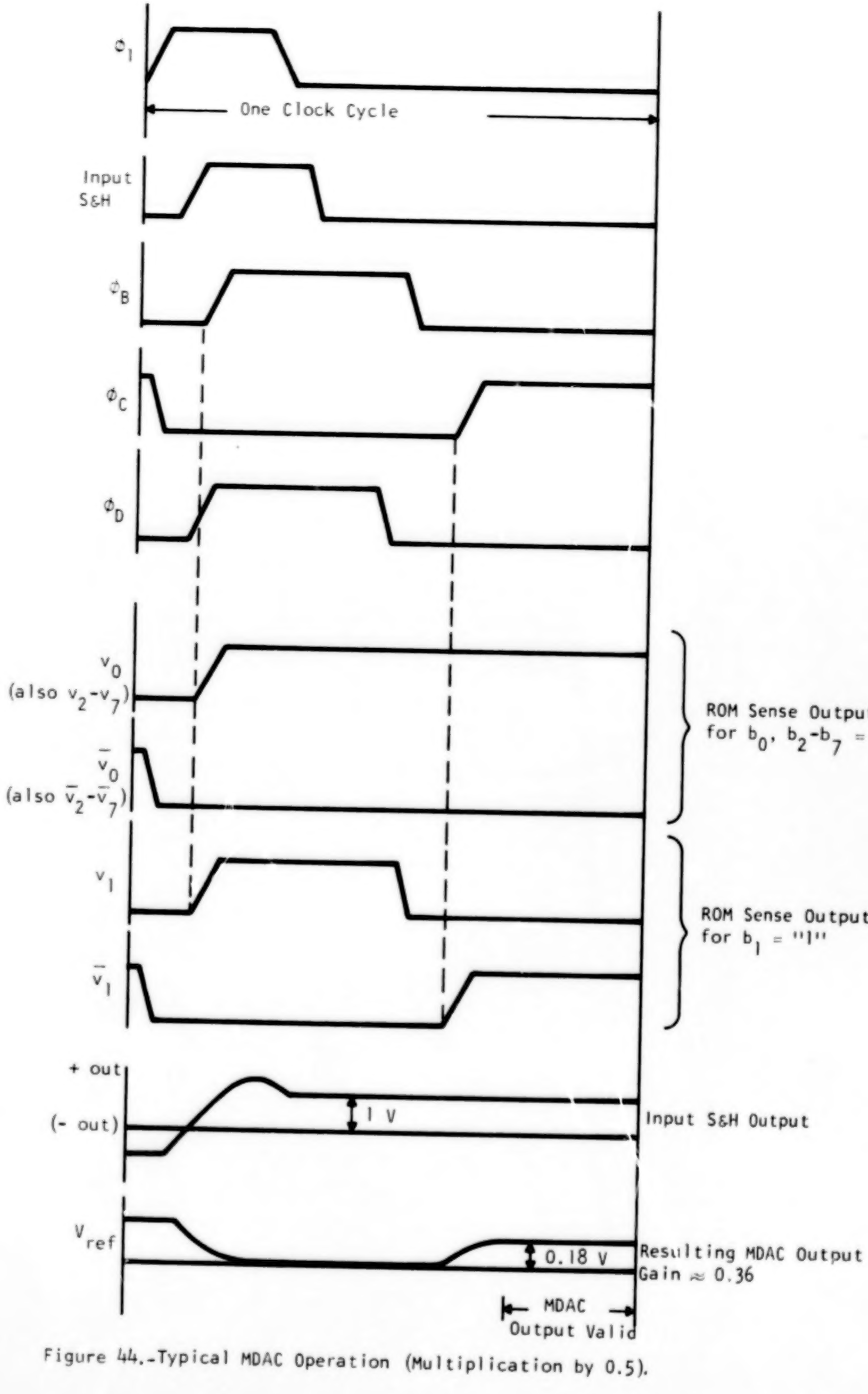

ϕ_1
One Clock Cycle
Input S&H
ϕ_B
ϕ_C
ϕ_D
v_0 (also v_2-v_7)
$\bar{v}_0$ (also $\bar{v}_2$-$\bar{v}_7$)
ROM Sense Outputs for b_0, b_2-b_7 = "0"
v_1
$\bar{v}_1$
ROM Sense Outputs for b_1 = "1"
+ out
(- out)
1 V
Input S&H Output
V_{ref}
0.18 V
Resulting MDAC Output Gain ≈ 0.36
MDAC Output Valid

Figure 44.-Typical MDAC Operation (Multiplication by 0.5).

2. Experimental Results

Figure 45 is a plot of the transfer curve for each side of the input sample-and-hold of Figure 42. The gain is 0.84, and the nonlinearity is very low (< 0.2% of input span). The input sample-and-hold circuitry functions properly for inputs of 1 to 7 V.

The MDACs were evaluated using the test setup shown in Figure 46. The MDAC was tested with both an external digital signal and chirps stored in internal ROM.

The evaluation of the MDAC using the sine chirp of the ROM is shown in Figure 47 and Table II. Figure 47 shows the response of the MDAC to a dc input and the sine chirp. Table II shows the word number, its binary code, and the analog value of the binary code for the sine chirp. The MDAC output voltages were normalized and compared to the analog representation of the code stored in the ROM.

The errors were found to be not more than ± 0.25 least significant bit (LSB), or one part in 512. Since the ROM is accurate to within ± 0.5 LSB, the worst-case error from the MDAC should be ± 0.75 LSB.

The MDAC was also tested using external digital words, and the relative accuracy is plotted in Figure 48. The differential nonlinearity was measured to be 0.25 LSB. Other parameters measured on the MDACs using external digital words were digital feedthrough , analog feedthrough, analog nonlinearity, and analog differential nonlinearity. The results of these tests are summarized in Table III.

E. Read-Only Memory (ROM) and ROM Address

1. Read-Only Memory

The on-chip ROM that supplies the cosine and sine chirp signals to the MDACs is illustrated in Figure 49. Two ROMs like the one shown are on the

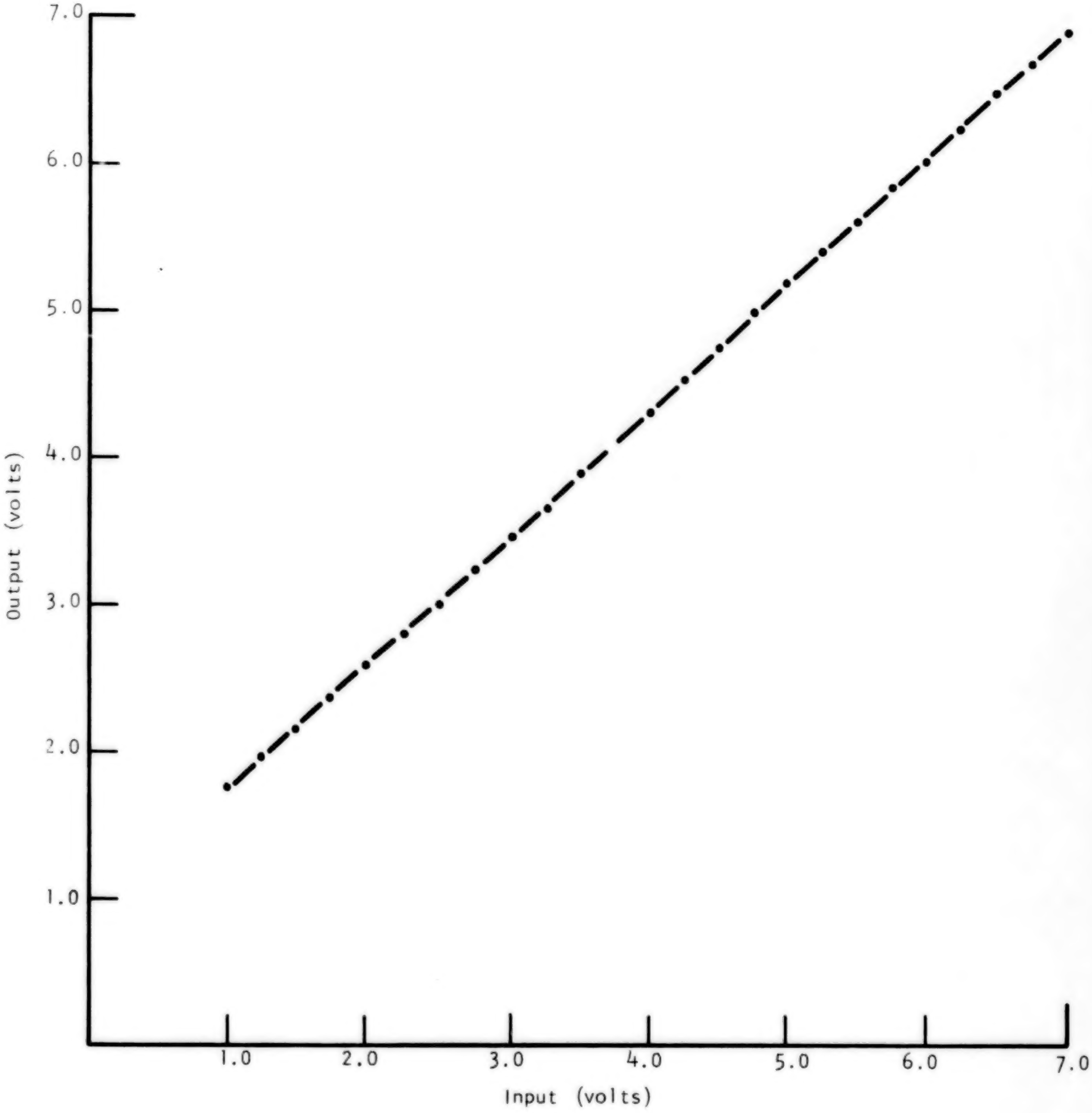


Figure 45.-Transfer Curve for Input Sample-and-Hold Circuit of MDAC.

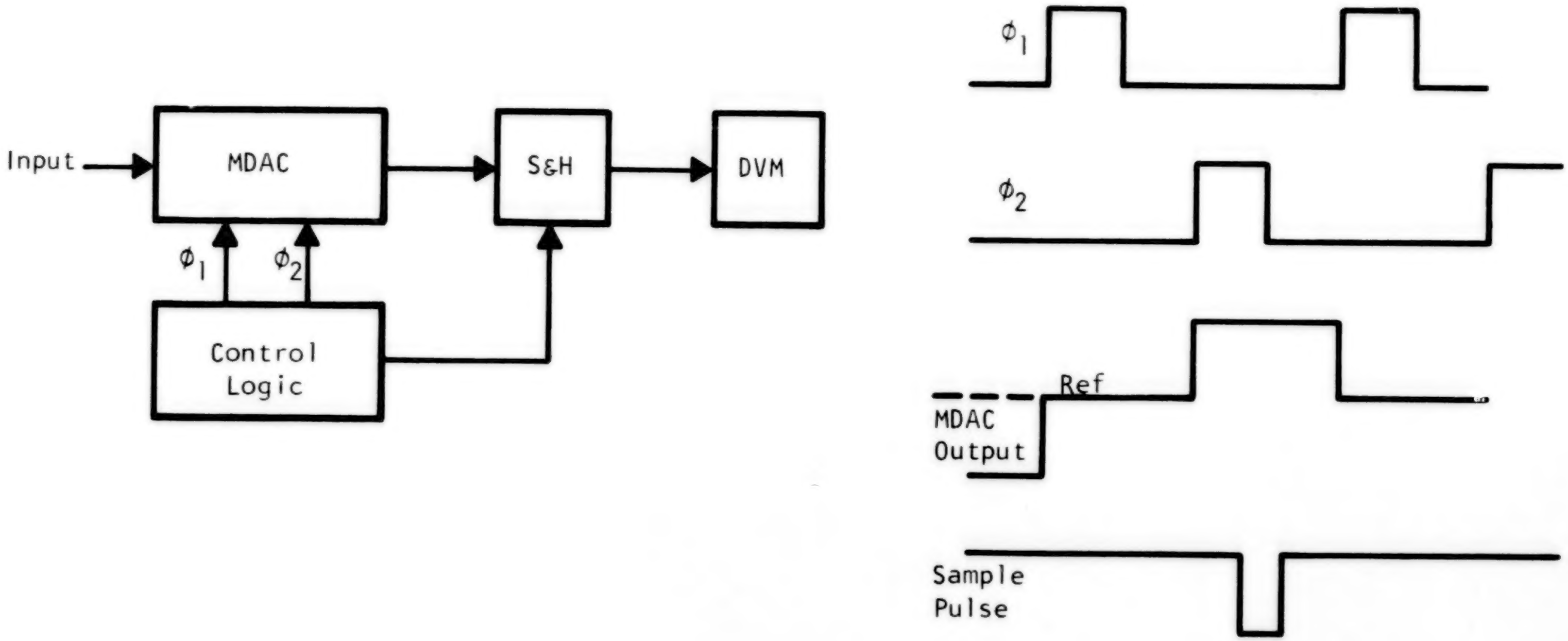

Input
MDAC
S&H
DVM
ϕ_1
ϕ_2
Control Logic
ϕ_1
ϕ_2
Ref
MDAC Output
Sample Pulse

Figure 46.- Block Diagram of MDAC Test.

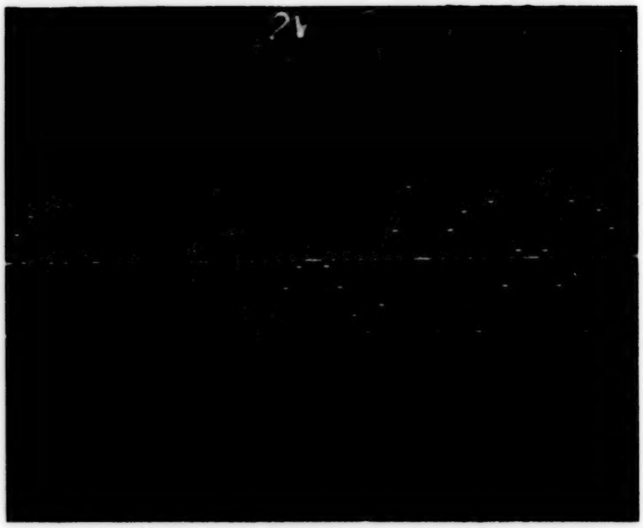


Figure 47.-Response of MDAC to dc Input and Sine Chirp of Internal Rom $(V^+ - V^-) < 0$.

TABLE II

MDAC ERROR

Word Number	Binary Code	Analog Value	MDAC Output*	Error†
0	00000000	0.0000	0.0000	0
1	00001100	0.0945	0.0951	0.077
2	00110001	0.3858	0.3870	0.154
3	01100010	0.7717	0.7725	0.103
4	01111111	1.0000	1.0000	0.000
5	01010001	0.6378	0.6388	0.128
6	11001111	-0.3858	-0.3843	0.192
7	10000010	-0.9921	-0.9933	0.154
8	00000000	0	0.0009	0.115
9	01111110	0.9921	0.9920	0.013
10	11001111	-0.3858	-0.3844	0.179
11	10101111	-0.6378	-0.6373	0.064
12	01111111	1.0000	1.0004	0.051
13	10011110	-0.7717	-0.7715	0.026
14	00110001	0.3858	0.3872	0.179
15	11110100	-0.0945	-0.0938	0.090
16	00000000	0.0000	-0.0002	0.026

*Normalized

†Fraction of LSB

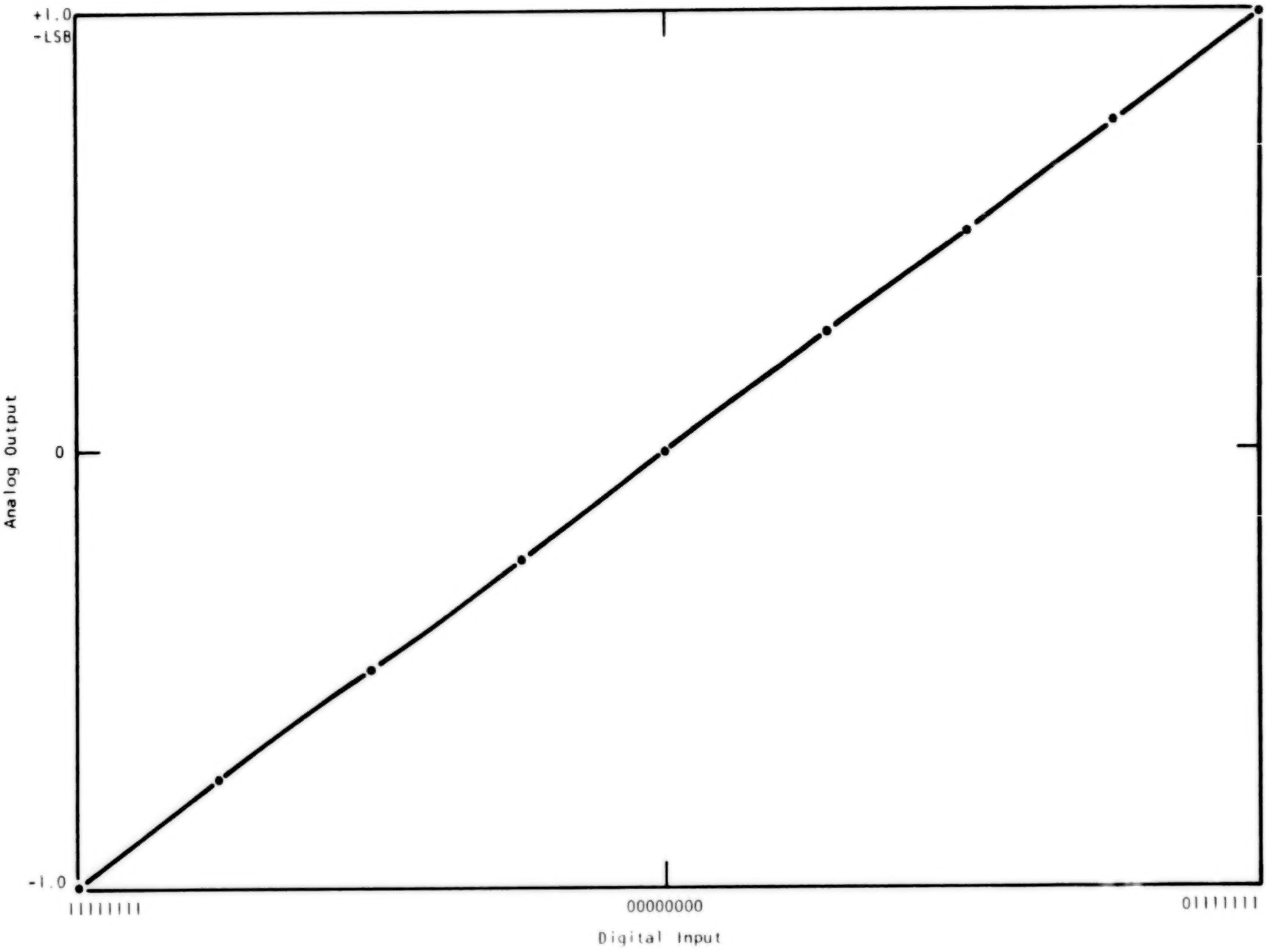


Figure 48.- Relative Accuracy of MDACs.

TABLE III

MDAC CHARACTERISTICS

Analog Nonlinearity(1)	0.2% of input span
Analog Feedthrough(2)	< 0.5 mV at 100 kHz
Analog Differential Nonlinearity(3)	± 0.25 LSB
Digital Feedthrough(4)	± 1.25 mV

(1) Measured by holding digital input constant and varying the analog input.

(2) Variable analog input with digital word programmed for zero gain.

(3) Maximum deviation of any bit size from theoretical value of 1 LSB.

(4) Variable digital word with analog input held at zero.

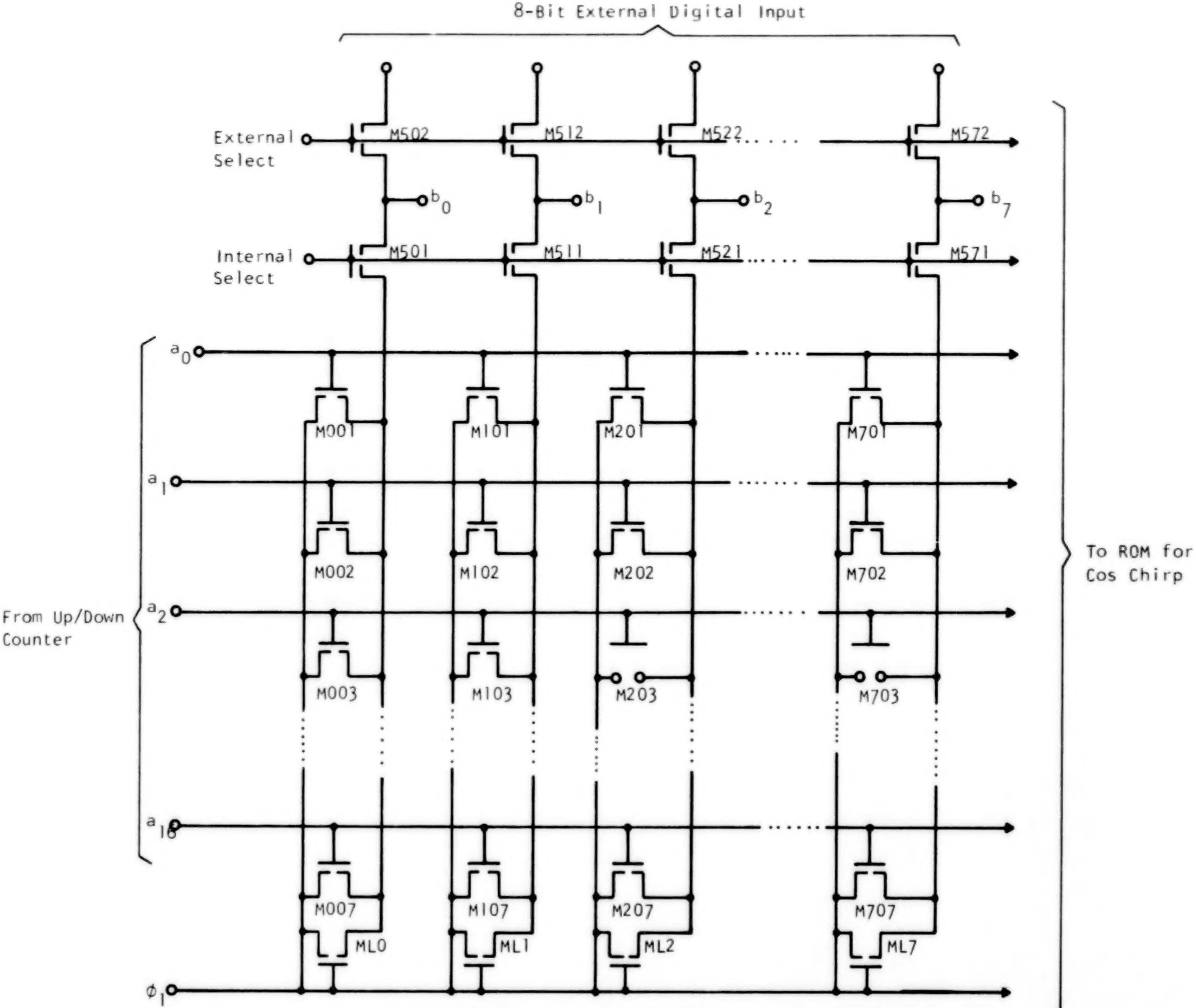

8-Bit External Digital Input
External Select
Internal Select
M502
M512
M522
M572
b0
b1
b2
b7
M501
M511
M521
M571
a0
a1
a2
a16
From Up/Down Counter
M001
M101
M201
M701
M002
M102
M202
M702
M003
M103
M203
M703
M007
M107
M207
M707
ML0
ML1
ML2
ML7
φ1
To ROM for Cos Chirp

Figure 49.-8-Bit by 17-Word ROM (Sine Chirp Coded).

IC. One supplies the cos chirp and the other supplies the sine chirp. The outputs b_i are attached to the ROM sense circuit of Figure 43. These outputs can come from an external digital input by holding the external select line high and the internal select line low. To use the internal ROM, the internal select line is held high and the external select line is held low (to reduce capacitive loading of the ROM). There is actually a second set of internal/external select switches and outputs b_i on chip. Each set feeds a pair of MDACs. A photograph of the ROM is shown in Figure 50. It occupies an area of 0.62 mm^2 (35.5 x 27 mil^2).

The ROM shown consists of 17 eight-bit words. One word consists of a horizontal row of eight possible transistors in Figure 49. A bit is coded as a "0" or a "1" by the presence or absence, respectively, of a transistor. The ROM address lines a_j are fed by a 17-stage up/down ring counter. The ROM is addressed in an up/down manner since the 32-point chirp is symmetrical about the seventeenth point. Each word, j, is addressed sequentially by pulling the appropriate address line to a high voltage. All other address lines are held low. ϕ_1 pulls the output lines b_i high, and when ϕ_1 falls, the output b_i will fall if there is a transistor in bit i of word j. If there is no transistor there, b_i will remain high. For example, if word two (line a_2) is addressed in Figure 49, outputs b_0 and b_1 will be low "0," and outputs b_2 and b_7 will be high "1". To illustrate the ROM timing, refer to Figure 44.

The appropriate address line, a_j, comes up and down with ϕ_D so that a_j is high when ϕ_1 falls. The ROM output is valid only after ϕ_1 has fallen. The fact that all ROM outputs are high when ϕ_1 is high insures that M204 of the ROM sense circuit will discharge the gate of M206 of Figure 41 once each cycle so that no excess charge can build up on this node.

A plot of the sine chirp coded in the ROM is shown in Figure 51. This plot can be compared to the photograph in Figure 47.

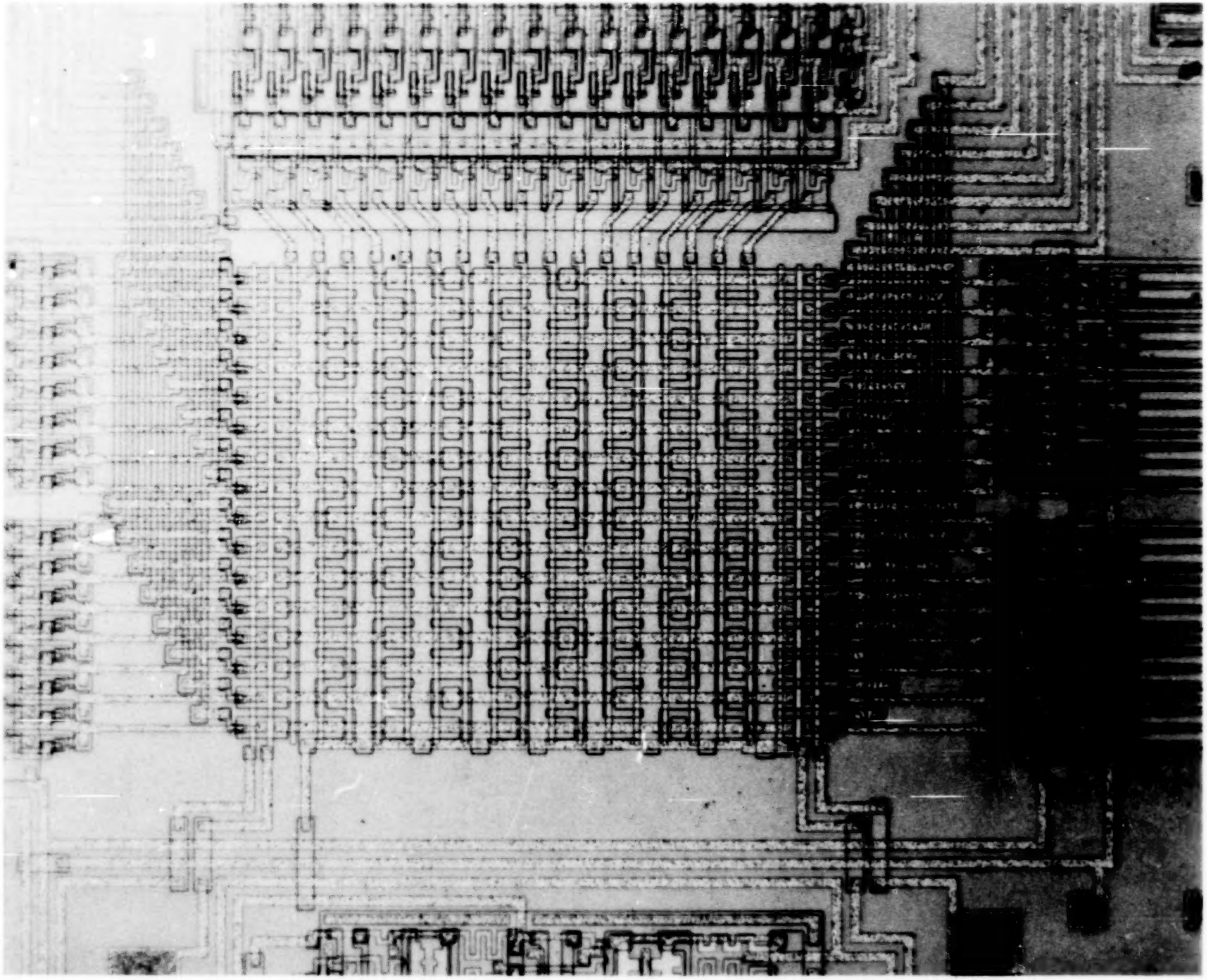


Figure 50.- Photograph of ROM.

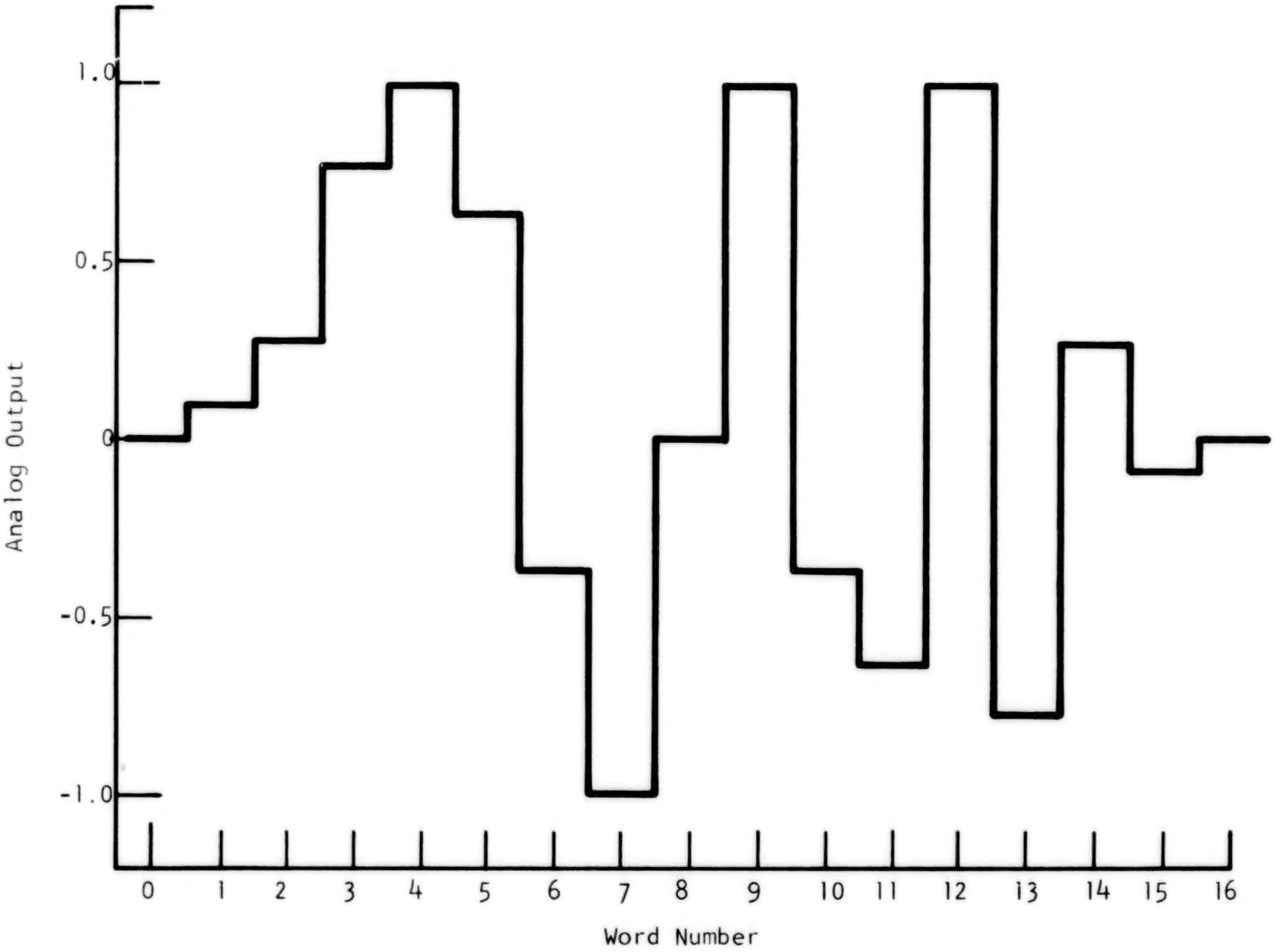


Figure 51.-Analog Representation of Sine Chirp Coded into ROM.

2. Up/Down Ring Counter (ROM Address)

The ROM address lines a_0 - a_{17} are fed by a 17-stage shift register that has the ability to reverse the shifting direction. A three-stage version of this circuitry is shown in Figure 52. Each basic shift register stage (one bit) is outlined in Figure 52. ϕ_1 and ϕ_2 are the nonoverlapping two phase clocks input to the IC. The basic shift register consists of two dynamic inverters with transmission gates, and its operation depends on charge storage. The operation of shift register 0 (SR0) of Figure 52 is illustrated in Figure 53. When ϕ_1 comes up, the 0.2 pF capacitor on node 2101 is charged to the level of the input to SR0 through M2100. Also, the 1 pF capacitor on the first inverter output node 2102 is charged to a high voltage through M2102. When ϕ_1 falls, node 2102 will discharge through M2101 if node 2101 is high; otherwise, node 2102 remains high. Thus, node 2102 is the inverse of the input to SR0. Next, ϕ_2 comes up, turning on M2103. If node 2102 is high, the charge on the 1 pF capacitor will divide between itself and the 0.2 pF capacitor on node 2103, and the voltage on node 2103 will be [1 pF/(1 pF + 0.2 pF)] v_0, where v_0 was the voltage on node 2102 before ϕ_2 turned M2103 on. If node 2102 is low when ϕ_2 comes up, any charge on node 2103 will discharge through M2101, since the gate of this transistor must be high. ϕ_2 also charges the 1 pF output capacitor on the second inverter output node 2104 through M2105. When ϕ_2 falls, node 2104 will remain high if node 2103 is low or will discharge through M2104 if node 2103 is high. Node 2103 is now isolated from 2102, since M2103 is off, allowing node 2102 to change without affecting the output node 2104. Thus, the voltage at the output of SR0 is that of the input delayed by one clock cycle.

To address the ROM properly, the shift register must shift one "1" back and forth across its 17 stages. This requires circuitry to detect the "1" when it reaches each end of the shift register and to reverse the transfer direction. It also requires circuitry to insure that only one stage of the shift register contain a "1," and that the other sixteen stages contain "0"s.

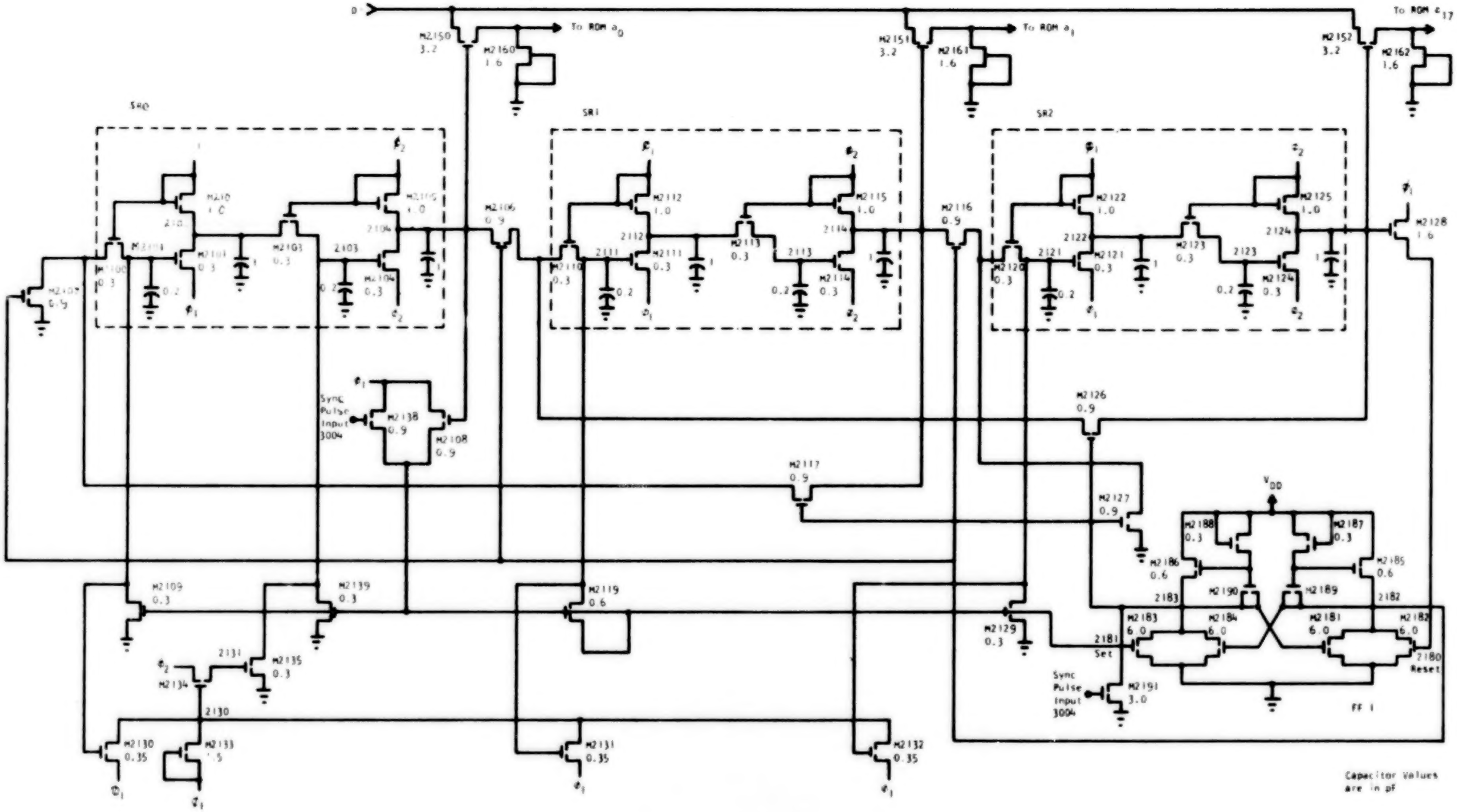

To ROM a_0
To ROM a_1
To ROM a_{17}
M2150 3.2
M2160 1.6
M2151 3.2
M2161 1.6
M2152 3.2
M2162 1.6
SR0
SR1
SR2
M2100 0.3
M2101 0.3
M2102 1.0
M2103 0.3
M2104 0.3
M2105 1.0
M2106 0.9
M2107 0.9
M2108 0.9
M2109 0.3
M2110 0.3
M2111 0.3
M2112 1.0
M2113 0.3
M2114 0.3
M2115 1.0
M2116 0.9
M2117 0.9
M2119 0.6
M2120 0.3
M2121 0.3
M2122 1.0
M2123 0.3
M2124 0.3
M2125 1.0
M2126 0.9
M2127 0.9
M2128 1.6
M2129 0.3
M2130 0.35
M2131 0.35
M2132 0.35
M2133 1.5
M2134
M2135 0.3
M2138 0.9
M2139 0.3
M2181 6.0
M2182 6.0
M2183 6.0
M2184 6.0
M2185 0.6
M2186 0.6
M2187 0.3
M2188 0.3
M2189
M2190
M2191 3.0
2102
2103
2104
2111
2112
2113
2114
2121
2122
2123
2124
2130
2131
2180 Reset
2181 Set
2182
2183
Sync Pulse Input 3004
V_{DD}
FF 1
ϕ_1
ϕ_2
0.2
1
Capacitor Values are in pF

Figure 52.-Three-Stage Up/Down Ring Counter.

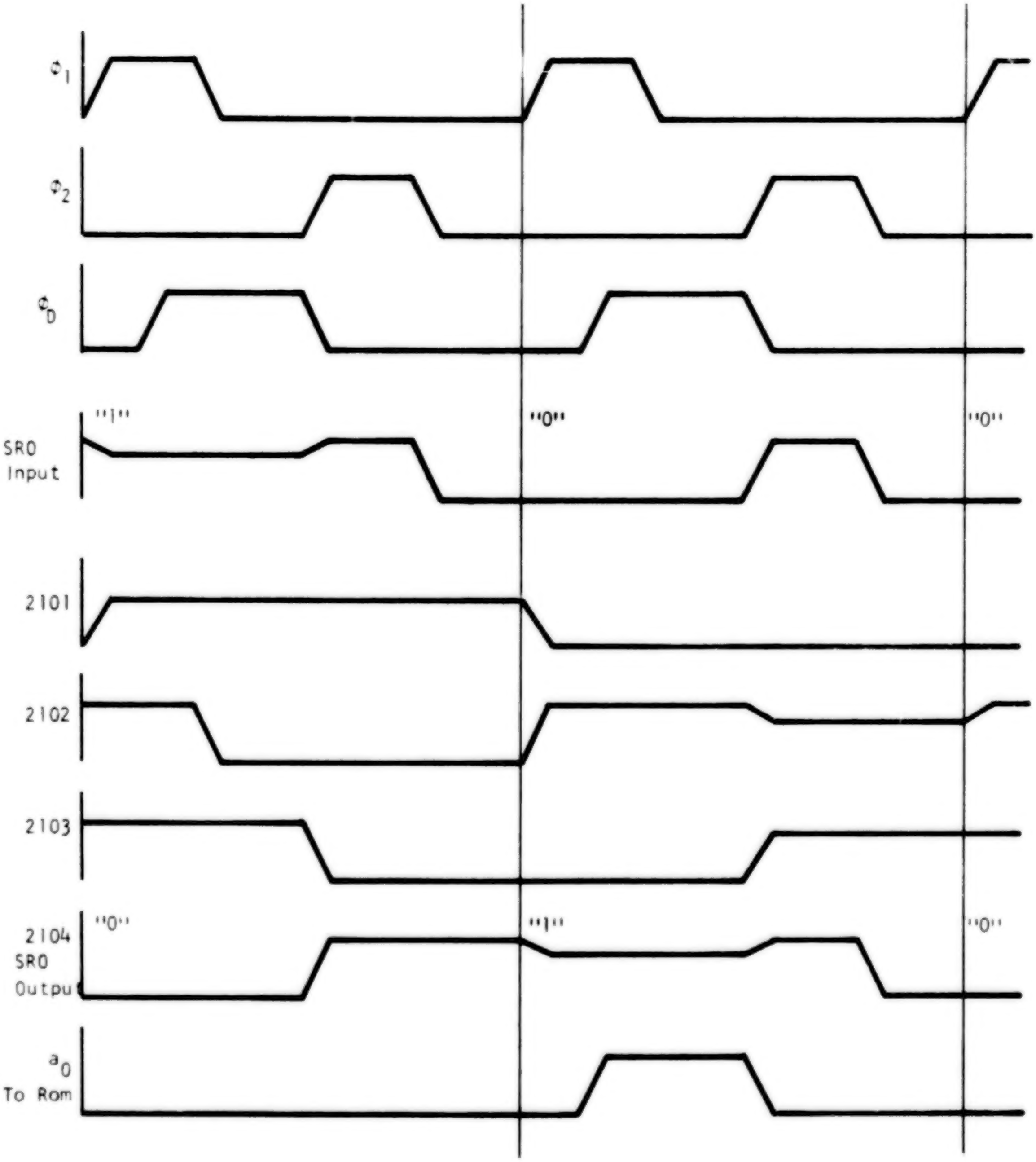

ϕ_1
ϕ_2
ϕ_D
"1"
"0"
"0"
SRO Input
2101
2102
2103
"0"
"1"
"0"
2104 SRO Output
a_0 To Rom

Figure 53.-Typical Shift Register Operation (SRO). Capacitive coupling, time delays, and MOSFET thresholds ignored. Previous SRO inputs have been "0"s.

The shift register must also have circuitry to synchronize it with an external pulse.

The direction of transfer is determined by the state of the static S-R flip-flop FF1. With flip-flop output node 2182 high and node 2183 low, the feed-forward transmission gates M2107, M2106, and M2116 are on, and the feedback transmission gates M2127, M2126, and M2117 are off. The output of each stage of the shift register is electrically connected to the input of the next stage, and transfer is in the forward direction. When the "1" reaches the final stage of the shift register, transistor M2128 will be on and the reset node 2180 will come up and down with ϕ_1. This causes the flip-flop to change state, and the feed-forward transistors are turned off while the feedback transistors are turned on. Each stage's output is now electrically connected to the previous stage's input. Node 2111 rises to a high voltage, since it is now connected to node 2124. The "1" appears next at the output of the next-to-last stage (SR 1 in this example). "0"s are loaded into the last stage by M2127, which is tied to ground. Transfer continues in the reverse direction until the "1" reaches the output of the first stage. Then when ϕ_1 comes up, M2108 is on and the set node 2181 comes up and down, causing the flip-flop to change stage again. The feed-forward transistors are now on, and the feedback transistors are off. The "1" next appears at the output of the second stage. "0"s are loaded into the first stage by M2107, which is connected to ground.

To insure that the shift register contains only one "1," two cases must be considered. The first case is that when power is supplied to the circuit, the shift register contains one or more "1"s. In this case, the output of the first stage of the shift register will eventually be high. When this occurs, M2108 will be on, and node 2181 will come up and down with ϕ_1. This sets the inputs to each stage of the shift register low through M2109 and M2129, except for the second stage, which is set high by M2119. At the end of this clock cycle only the second shift register contains a "1," and transfer is in the forward direction.

The second case is that when power is supplied to the circuit, the shift register contains all "0"s. In this case, a 17-input dynamic NOR circuit sets the first stage to "1." The NOR circuit consists of transistors M2130 - M2133, in Figure 52, Node 2130 is pulled high with ϕ_1. If the input to any stage is high, node 2130 falls with ϕ_1, since at least one of the transistors M2130 - M2132 is on. If the inputs to all stages are low, then all transistors M2130 - M2132 are off, and node 2130 will remain high. This leaves M2134 on. Node 2131 will then come up and down with ϕ_2. This discharges node 2103 through M2135 so that when ϕ_2 falls, the output of the first stage, node 2104, will remain high or "1." After this occurs, the shift register contains a "1," and node 2131 should never come up again. Node 2130, however, will rise and fall with ϕ_1 every clock cycle.

Three transistors, M2138, M2139, and M2191, are added to the circuit of Figure 52 to synchronize the counter with a sync pulse (M2119 is also only necessary for synchronization). The sync pulse is derived from another circuit. When it occurs, it comes up with ϕ_1 and down with the rising edge of ϕ_2. The set node 2181 is pulled up with ϕ_1, since M2138 is on. This resets the inputs of all stages except the second low through M2109 and M2129. The second stage input is set high by M2119. Also, node 2103 is discharged by M2139 so that M2104 will not sink current from node 2111 to ground. The sync pulse is also applied to the gate of M2191 to make sure that the flip-flop comes up in the forward transfer state (node 2182 high). This transistor is necessary because it is possible for the reset pulse to occur when a "1" is in the last stage, in which case the reset line 2180 would also come up and down with ϕ_1. Since the sync pulse remains high after ϕ_1 is low again, the flip-flop will be set in the proper stage. At the end of the clock cycle, the output of the second stage will be "1," and the shift register will be transferring in the forward direction. (M2191 is necessary only to guarantee synchronization after the first sync pulse. This is not required here. If M2191 were removed, synchronization would be guaranteed after the second sync pulse.)

The shift register outputs go to the gates of transistors M2150 - M2152, which allow ϕ_D to pull up the ROM address line attached to the transistor whose gate is high. The depletion devices (M2160 - M2162) are attached to the ROM address lines to keep capacitive coupling in the ROM from pulling the other address lines up. The depletion device on the address line that is high will sink 0.6 mA of current from ϕ_D. The ϕ_D driver is able to supply this current with very little drop in output voltage. The output pulse is illustrated in Figure 53. Figure 54 illustrates the counter in normal operation (i.e., one "1" bit, counter synchronized to sync pulse 3004 if it exists). It shows the first and last shift register outputs, the first and last ROM outputs, the relationship to the sync pulse, and the S-R flip-flop inputs and outputs. The flip-flop FF1 consists of a pair of static inverters with bootstrapped loads. M2187 and M2188 keep the gates of M2185 and M2186 from falling below a threshold below V_{DD}. M2189 and M2190 are gated capacitors that bootstrap the gates of M2185 or M2186 when the output 2182 or 2183 starts to come up. This turns the load devices on hard, decreasing the rise time and allowing the output voltage to reach V_{DD}. The set and reset transistors M2183 and M2182 are in parallel with the driver devices M2184 and M2181.

A photograph of the up/down counter is shown in Figure 55. Its area is approximately 0.75 mm^2 (40 x 29 mil^2).

3. Synchronization

To operate two or more ICs together, the up/down counters must be synchronized to each other. It is required that the counter of an IC be 180° out of phase with the counter it is synchronized to. One cycle of the chirp z-transform algorithm consists of 64 clock cycles. Therefore, when two ICs are operated together, one should be on count 32 (t_{32}) when the other is on count 0 (t_0).

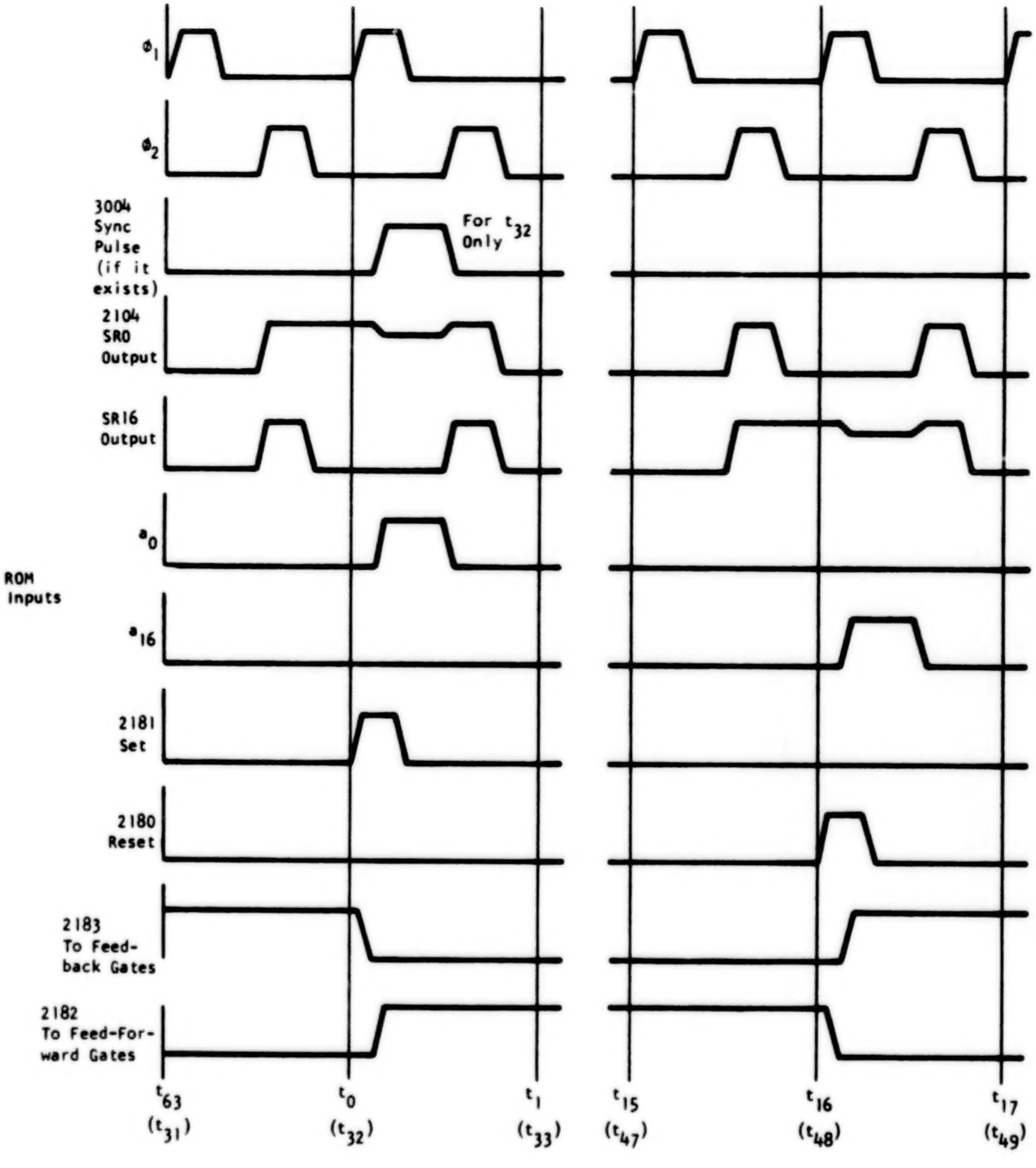

ϕ_1
ϕ_2
3004 Sync Pulse (if it exists)
For t_{32} Only
2104 SRO Output
SR16 Output
ROM Inputs
a_0
a_{16}
2181 Set
2180 Reset
2183 To Feed-back Gates
2182 To Feed-For-ward Gates
t_{63} (t_{31})
t_0 (t_{32})
t_1 (t_{33})
t_{15} (t_{47})
t_{16} (t_{48})
t_{17} (t_{49})

Figure 54.- Up/Down Counter Waveforms - Normal Operation (Sychronized to 3004).

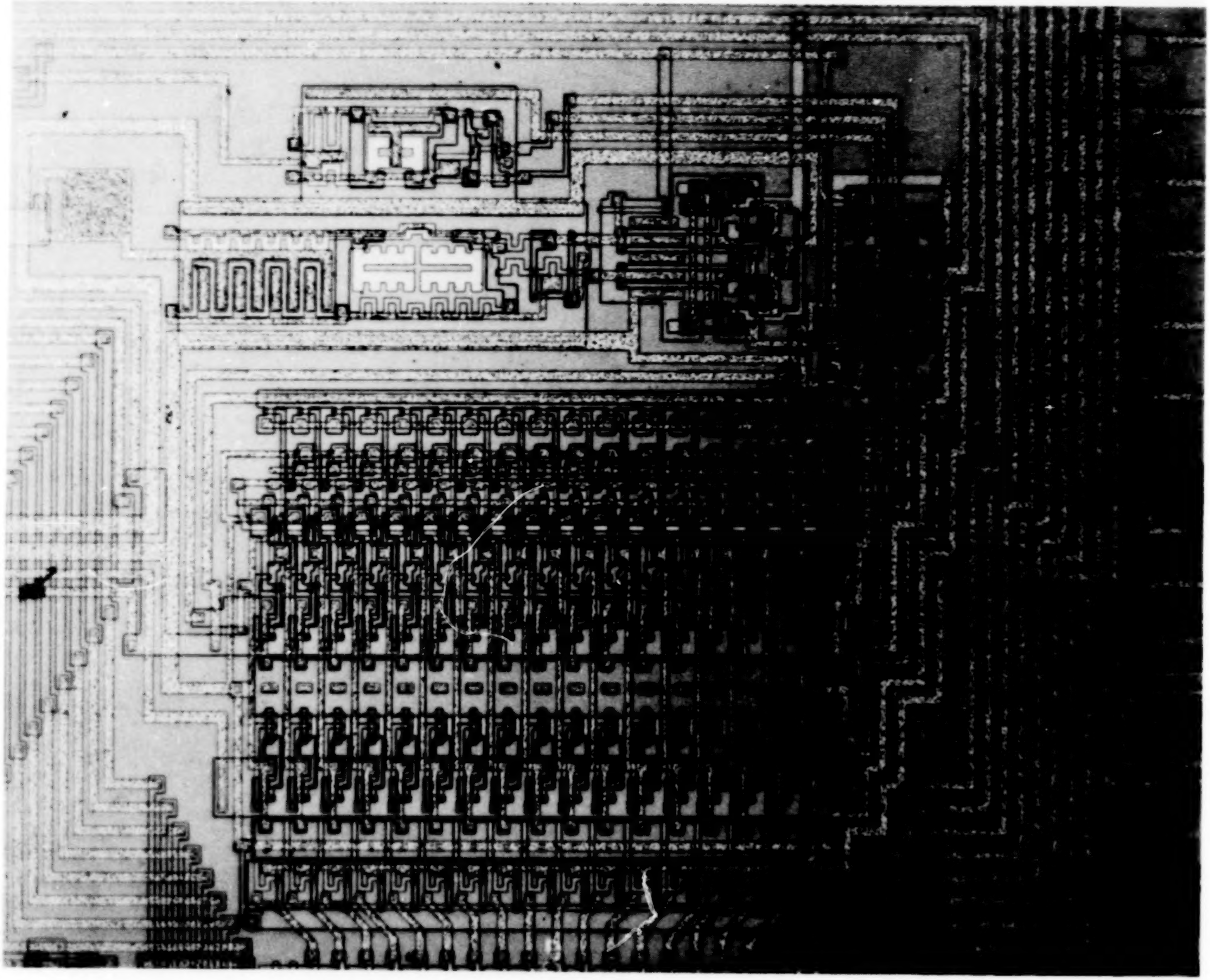


Figure 55.- Photograph of Up/Down Counter.

In order to obtain this synchronization, each counter must have an external sync pulse output to provide a pulse to the other IC, and a sync pulse input to accept a pulse for synchronization to another IC. The output sync pulse is a square wave. The sync pulse input circuit accepts the square wave output from another IC and converts this to an internal pulse (3004) with duration of less than one clock cycle to reset the counter and external sync pulse generation (refer to Figures 52 and 54). The relationship of the sync pulses for two synchronized chips is illustrated in Figure 56. Also shown is the relationship of the sync pulses to the flip-flop FF1 (Figures 52 and 54) output (2182) to the feed-forward transistors in the up/down counter. It can be seen that the up/down counters of the two ICs that have a period of 32 clock cycles are in phase, and the sync pulse output of the second IC is 180° out of phase with that of the first stage. The external sync pulse generator is shown in Figure 57. The circuit uses a set/rest flip-flop (identical to FF1 in the up/down counter) and seven more transistors to implement a toggle flip-flop that changes state each time a pulse appears on the set line 2181 to FF1. This occurs once every 32 clock cycles in normal operation. The basic RS flip-flop consists of the unmarked transistors in Figure 57. Figure 58 illustrates the circuit's operation. Assume the output 2282 is low and 2283 is high. Then node 2286 will be low and node 2287 will be high, since ϕ_2 will have turned M2289 and M2290 on and off. Node 2181 will come up and down with ϕ_1 every 32 clock cycles. With the flip-flop in the above state, M2292 is on, and node 2281 will come up and down with the input node 2181. M2291 is off and node 2280 stays low. This causes the flip-flop to change state. The transistor M2293 is on during this process to keep node 2280 from being pulled up by capacitive coupling to the flip-flop. M2294 is off. Now output 2282 is high and 2283 is low. When ϕ_2 comes up, node 2287 discharges through M2290, and node 2286 charges through M2289. The circuit is triggered during synchronization so that the output waveform at 2282 is 180° out of phase with the sync pulse. The duration of the internal sync pulse (3004) is longer than that of 2181, so that sync is assured. The

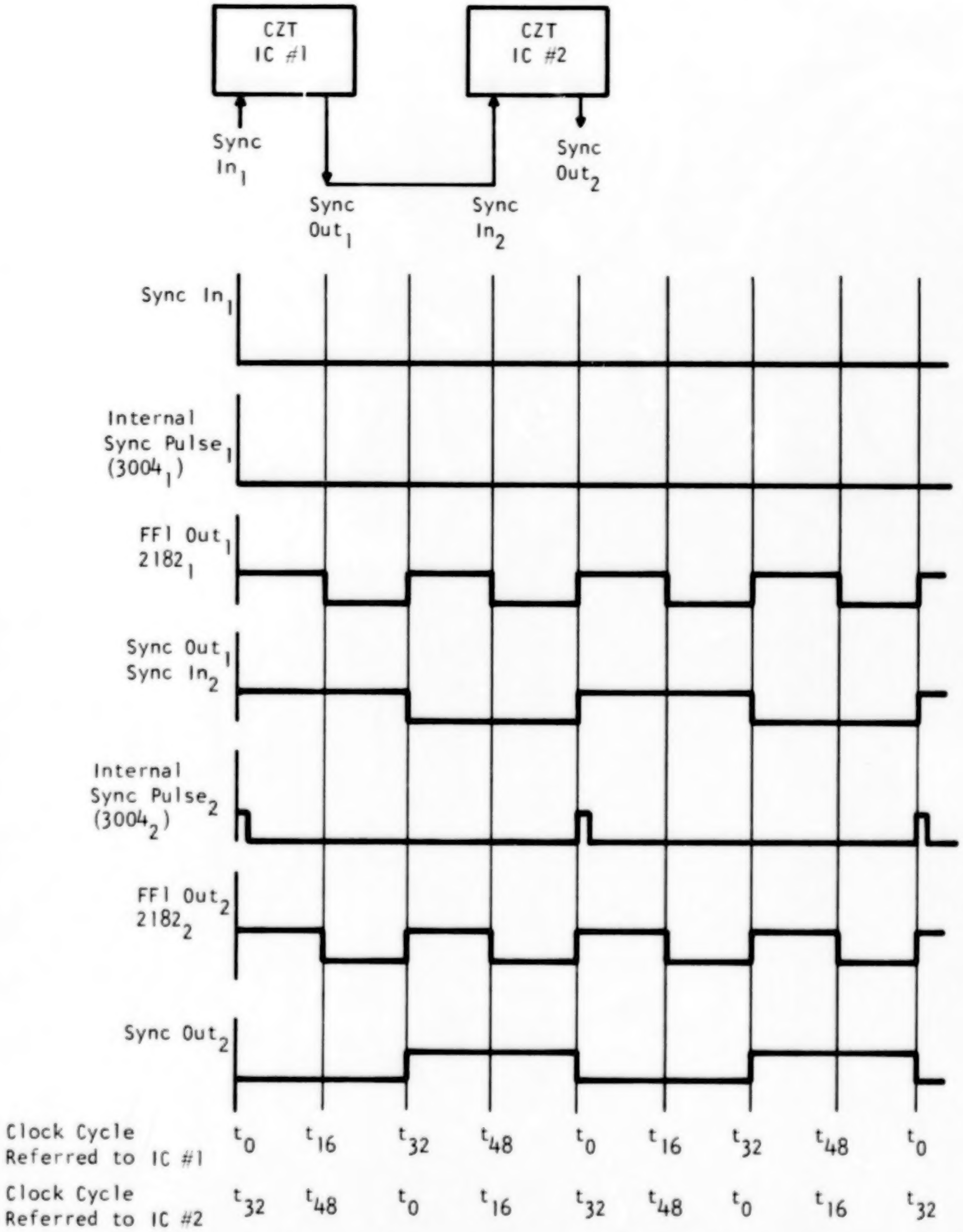
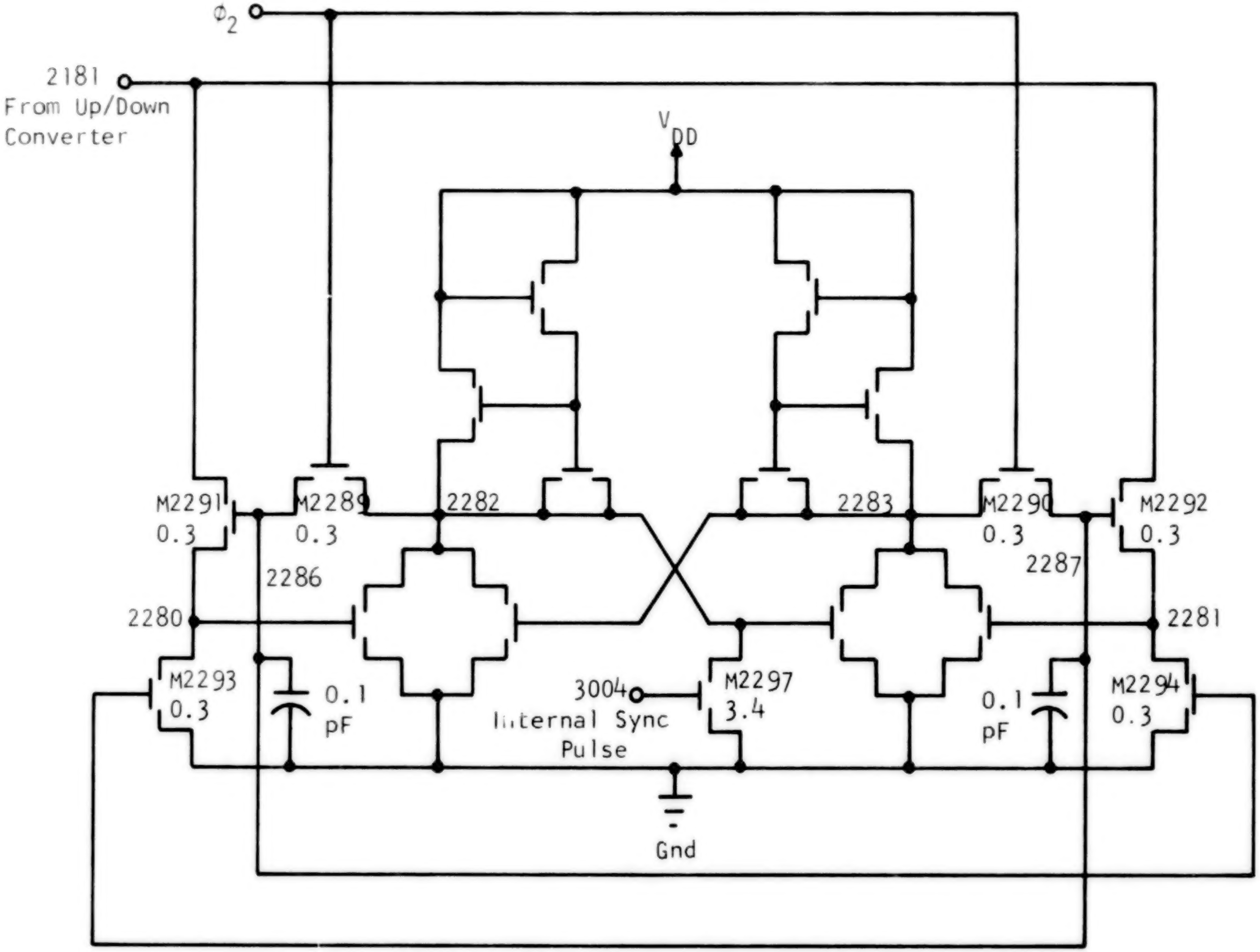
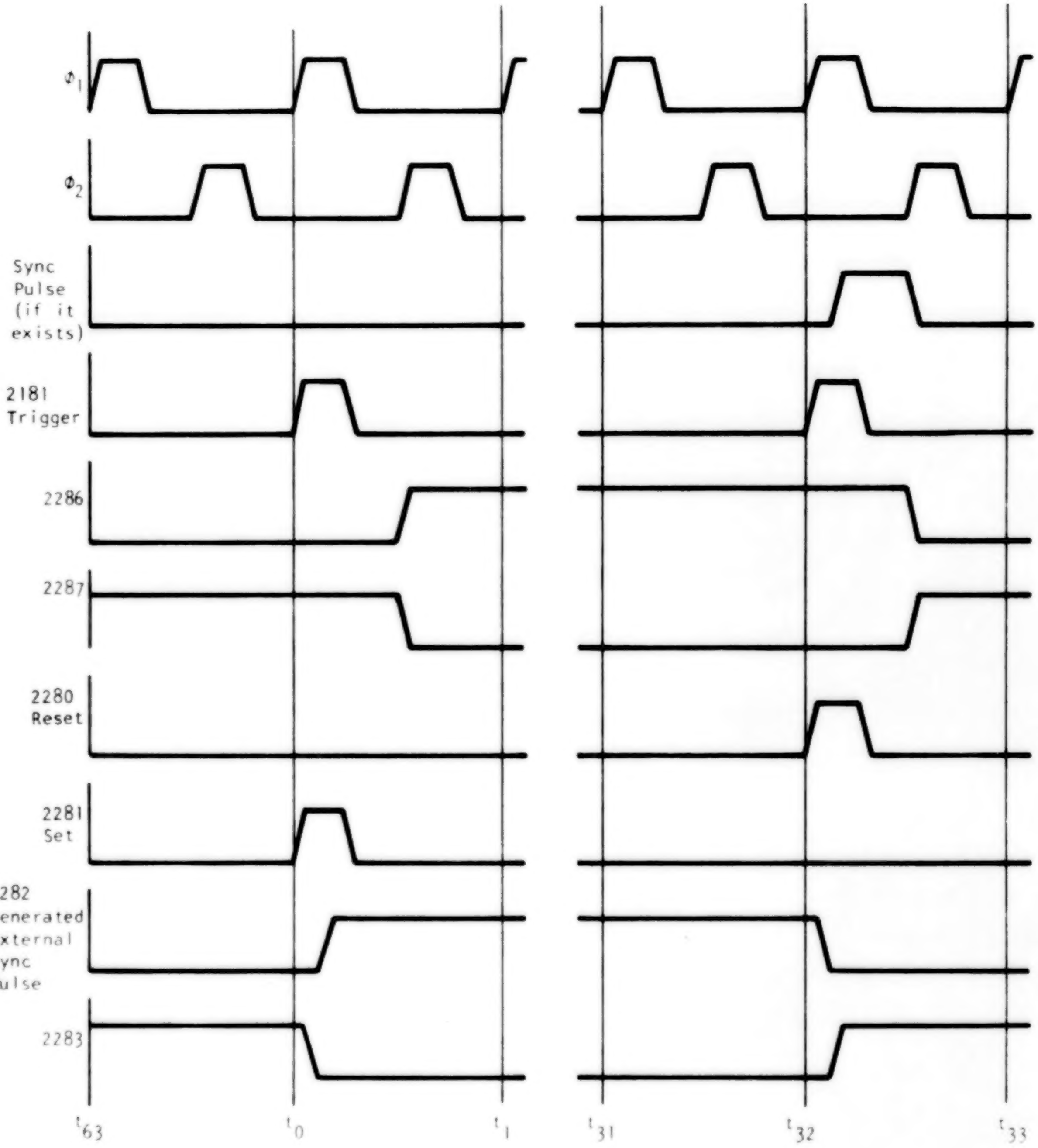

CZT
IC #1
CZT
IC #2
Sync In1
Sync Out1
Sync In2
Sync Out2
Sync In1
Internal Sync Pulse1 (3004₁)
FF1 Out1 2182₁
Sync Out1 Sync In2
Internal Sync Pulse2 (3004₂)
FF1 Out2 2182₂
Sync Out2
Clock Cycle Referred to IC #1
t0 t16 t32 t48 t0 t16 t32 t48 t0
Clock Cycle Referred to IC #2
t32 t48 t0 t16 t32 t48 t0 t16 t32

Figure 56.-Synchronization of Two CCD CZT ICs.



ϕ_2
2181
From Up/Down
Converter
V_{DD}
M2291
0.3
M2289
0.3
2282
2283
M2290
0.3
M2292
0.3
2286
2287
2280
2281
M2293
0.3
0.1
pF
3004
Internal Sync
Pulse
M2297
3.4
0.1
pF
M2294
0.3
Gnd

Figure 57.-External Sync Pulse Generator.



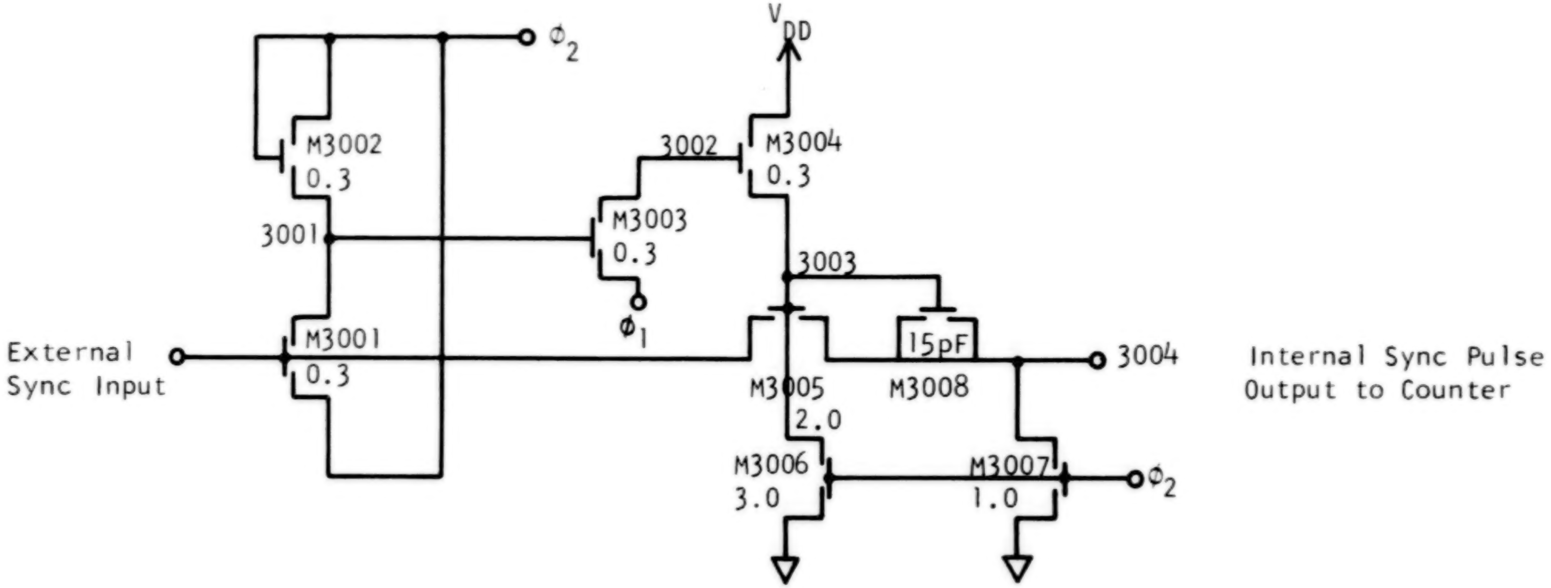
Φ_1
Φ_2
Sync Pulse (if it exists)
2181 Trigger
2286
2287
2280 Reset
2281 Set
2282 Generated External Sync Pulse
2283
t_{63}
t_0
t_1
t_{31}
t_{32}
t_{33}

Figure 58.- External Sync Pulse Generator Timing - Normal Operation (Synchronized to 3004).

relationship of the internal sync pulse (3004) to the generated external sync pulse is shown in Figure 58 during normal operation. It is out of phase with node 2282. The actual sync pulse generated for use off-chip comes from a driver that will be discussed later. The inputs to the driver are 2282 and 2283, and the output waveform is that of node 2282 with slightly more rise and fall time delays. This driver is necessary to drive the larger capacitance associated with going off-chip. The output pulse is called T_2.

The circuit used to generate the short internal sync pulse from an applied external sync squarewave is called GEN30 and is shown in Figure 59. Figure 60 illustrates its operation. When the external sync input is low, node 3001 remains high after ϕ_2 falls. Node 3002 comes up and down with ϕ_1 every clock cycle, and node 3003 is charged to a threshold below V_{DD}. When the external input comes up (which will be with ϕ_1 plus a small delay), the output node 3004 comes up immediately, since M3003 is on. The gate of M3005 is bootstrapped by M3008 so that 3004 reaches the full potential of the input. Node 3001 falls immediately with the input rising edge, leaving 3002 floating high. When ϕ_2 comes up again, node 3001 comes up, allowing 3002 to discharge through M3003. M3006 and M3007 are turned on, turning off M3005 and pulling the output node 3004 down. The output cannot come up again until M3004 charges node 3003 high. This cannot occur until after the input external pulse falls. In this way, GEN30 generates a pulse with a duration of about $\frac{1}{2}$ clock cycle each time the external input comes up.

Figure 61 is a photograph of the sync outputs of two CZT ICs operating together. The sync output of one IC is fed into the sync input of the other. The sync output waveforms have a period 64 times that of the 10 kHz input clocks, ϕ_1 and ϕ_2. Note that the two sync outputs are 180° out of phase as in Figure 56.



ϕ_2
V_{DD}
M3002
0.3
3002
M3004
0.3
M3003
0.3
3001
3003
ϕ_1
External Sync Input
M3001
0.3
15pF
3004
Internal Sync Pulse Output to Counter
M3005
2.0
M3008
M3006
3.0
M3007
1.0
ϕ_2

Figure 59.-GEN 30 (Internal Sync Pulse).

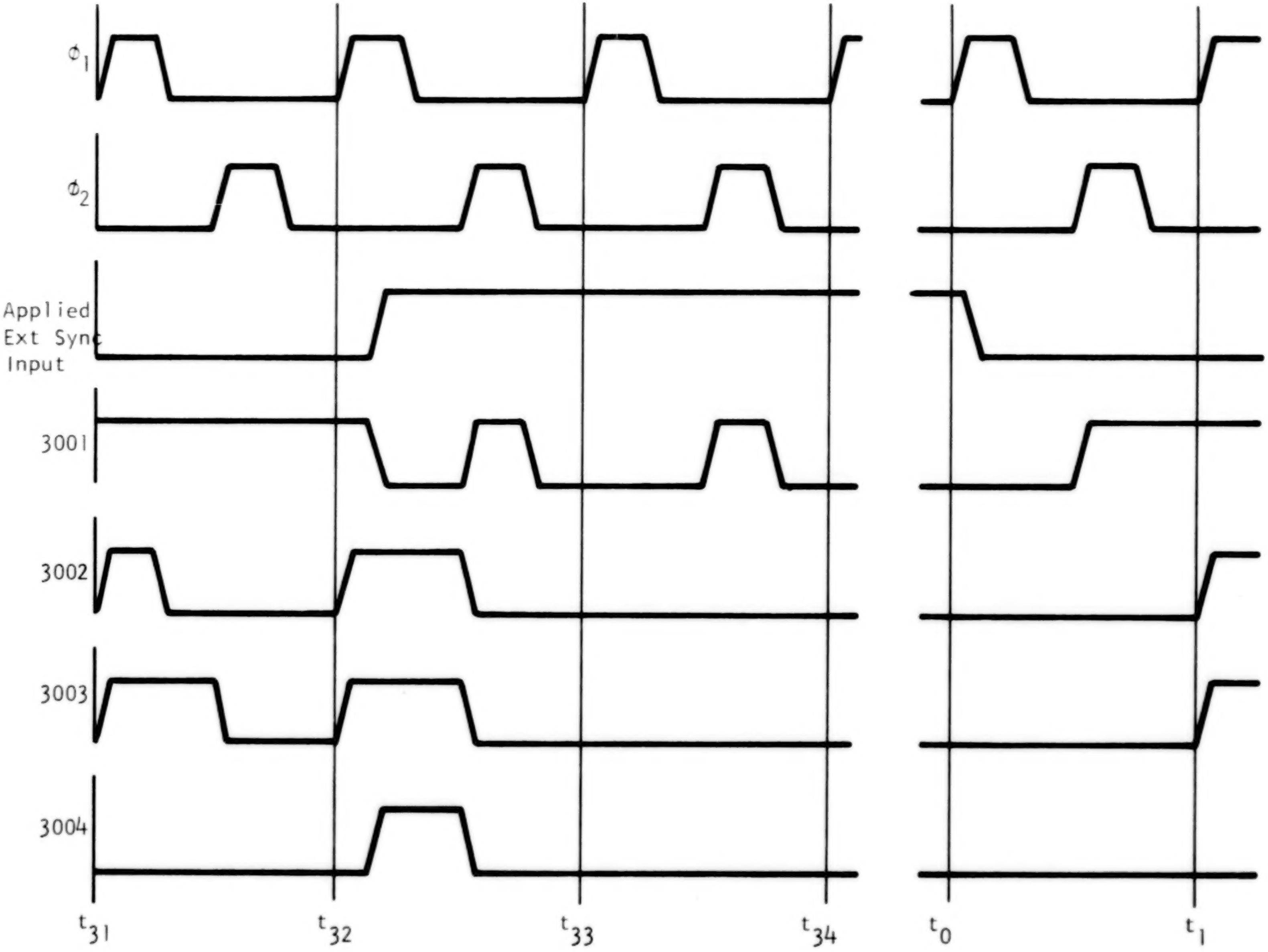

ϕ_1
ϕ_2
Applied Ext Sync Input
3001
3002
3003
3004
t_{31}
t_{32}
t_{33}
t_{34}
t_0
t_1

Figure 60.-GEN 30 Timing.

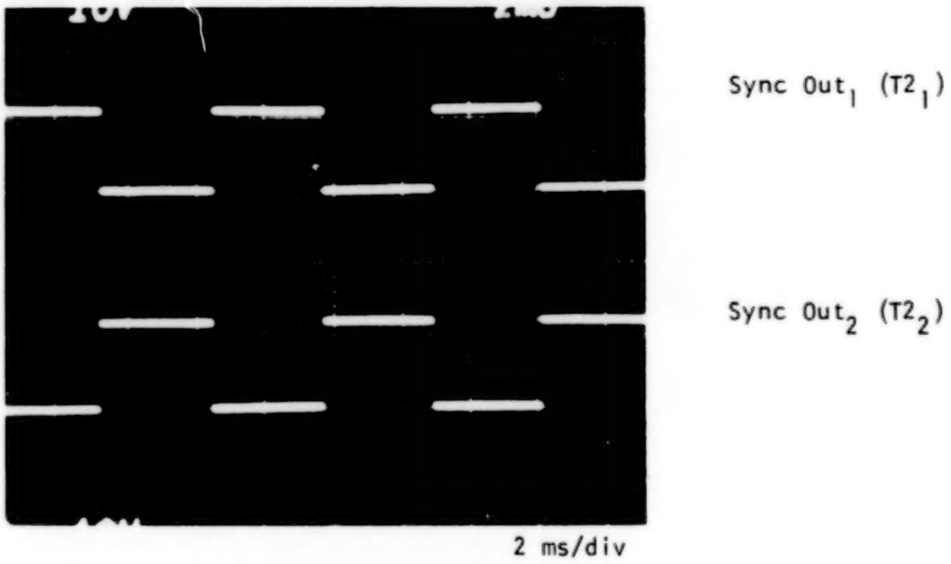


Figure 61.-Synchronization Outputs of Two CZT ICs Operating Together.

F. Timing Circuitry

1. Clock Generators

The derivation of the internal clocking pulses from the two-phase inputs ϕ_1 and ϕ_2 is illustrated in Figure 62. The 13 generators shown there use one or more of the circuits described below.

The first circuit will be referred to as G1 and is illustrated in Figure 63. This circuit configuration is used to produce most of the clock pulses. It requires a pullup pulse (node 4000) and a nonoverlapping pulldown pulse (node 4001). Assume that a pulldown pulse has occurred and the output (4006) and all internal nodes are low except for node 4003, which is high. When the pullup pulse occurs at node 4000, nodes 4002 and 4004 closely track the input. Nodes 4005 and 4006 are slightly delayed because 4003 is still high, keeping M4006 and M4008 on. Since 4005 is held down and 4004 rises quickly, the gated capacitor M4010 is charged to a level of $V_{DD} - V_T$. When 4002 has risen high enough to turn M4002 on, pulling node 4003 down, M4006 and M4008 are turned off. At this point nodes 4005 and 4006 begin rising rapidly, and node 4004 is bootstrapped by M4010 to a level $2(V_{DD} - V_T)$. This increases the rise times and allows the output node 4006 to reach V_{DD}. The time delays for the actual circuits used are typically 20 ns. The risetimes are typically 20 ns to 30 ns. When the pulldown pulse occurs at node 4001, node 4002 is pulled down, allowing 4003 to be pulled up while node 4004 is pulled down. Nodes 4005 and 4006 are then pulled down. The time delay before node 4006 starts down is typically 10 ns, and the fall time is typically 10 ns to 15 ns. The device sizes required for the G1 generator to produce 20 ns risetimes depend on the capacitive load it must drive. Typical designs set the W of M4009 in mils equal to the capacitive load in pF and the W of M4008 was set to 1.5 times that of M4009. The values of the other transistors depend on internal node capacitance ratios. Therefore, each G1 driver required a custom design.

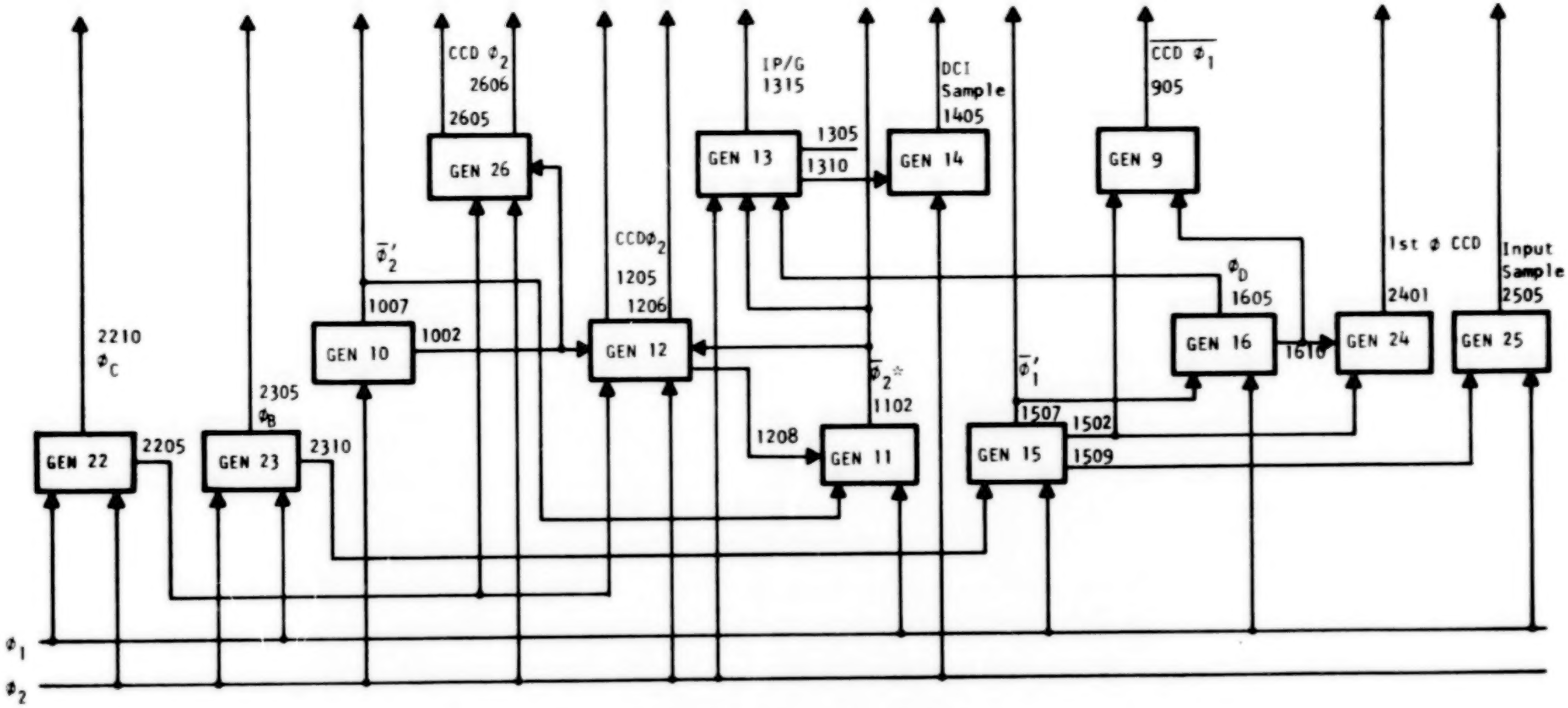

GEN 22
GEN 23
GEN 10
GEN 26
GEN 12
GEN 13
GEN 14
GEN 11
GEN 15
GEN 9
GEN 16
GEN 24
GEN 25
2210
ϕ_C
2205
2305
ϕ_B
2310
$\bar{\phi}_2'$
1007
1002
CCD ϕ_2
2606
2605
CCDϕ_2
1205
1206
1208
IP/G
1315
1305
1310
DCI
Sample
1405
$\bar{\phi}_2$*
1102
$\bar{\phi}_1'$
1507
1502
1509
$\overline{\text{CCD }\phi_1}$
905
ϕ_D
1605
1610
1st ϕ CCD
2401
Input
Sample
2505
ϕ_1
ϕ_2

Figure 62.-Block Diagram of Clock Generators.

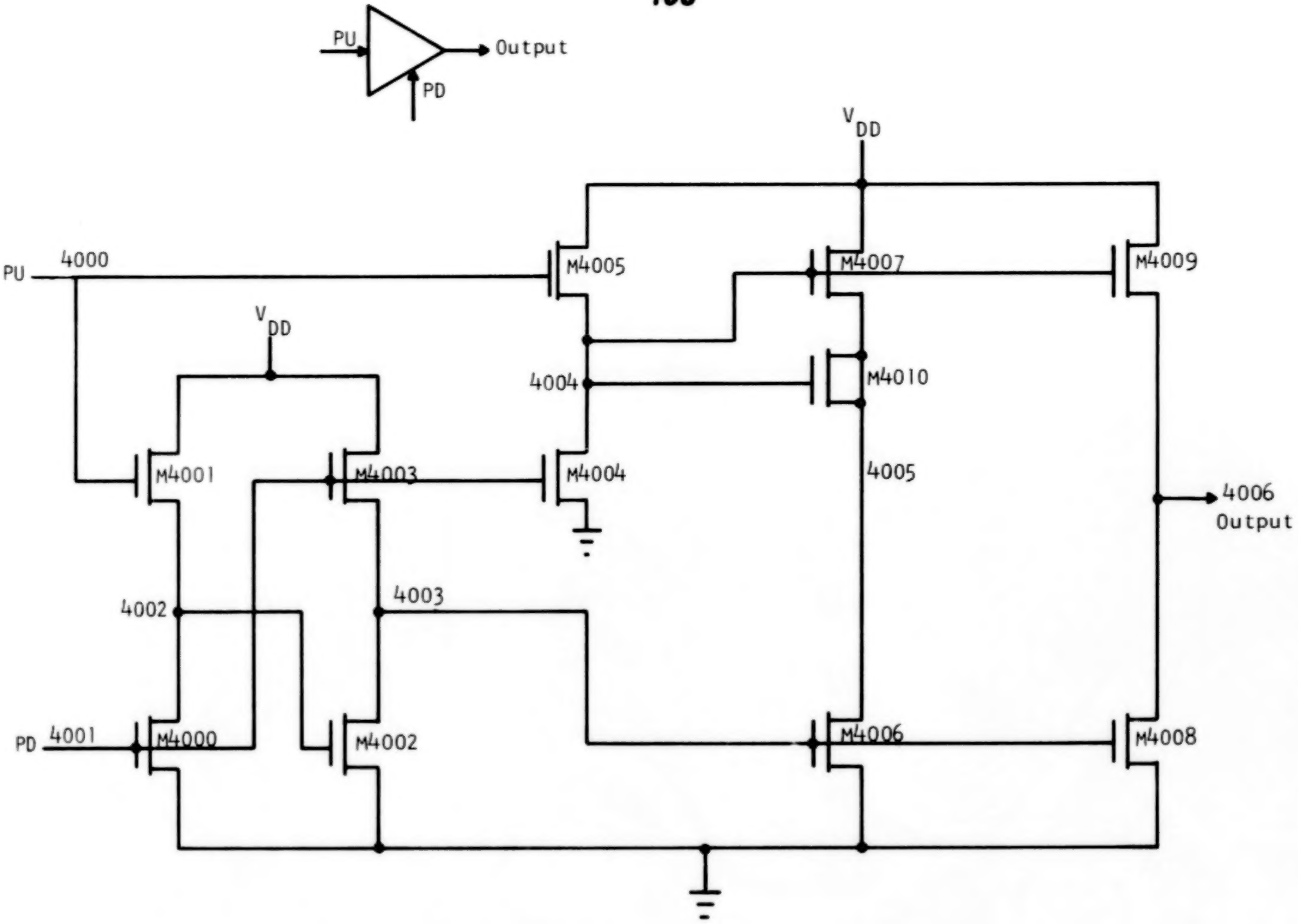

PU
Output
PD
V DD
PU
4000
M4005
M4007
M4009
V DD
4004
M4010
M4001
M4003
M4004
4005
4006
Output
4002
4003
PD
4001
M4000
M4002
M4006
M4008

Figure 63.-Gl Clock Pulse Generator.

A special version of the G1 driver is required to allow the CCD electrodes to float. This driver, G2, is shown in Figure 64. The difference between G2 and G1 is that the gate of M4004 on G2 is tied to a third pulse, which comes up when it is desired to float the outputs. The G2 driver also has a second pair of output transistors so that one generator drives two of the four CCD outputs. A second G2 generator drives the other two. The V_{DD} line to the second G2 generator can be trimmed to adjust for offsets in the DCIs.

The generator G3 shown in Figure 65 is a bootstrapped inverter circuit. The basic inverter consists of M4101 and M4102. M4103 keeps the gate of M4102 from falling below a threshold below V_{DD}. M4104 is a gated capacitor which bootstraps the gate of M4102 to a high voltage when the output node 4102 comes up. This speeds up the risetime by turning M4102 on hard. The generator G4 is an inverter whose pullup transistor is not bootstrapped. It is shown in Figure 66.

Figure 67 shows the generator G5. G5 produces a short pulse at node 4204 from a longer trigger pulse at node 4200. Before the trigger pulse occurs, node 4002 is pulled up by a set pulse on node 4201. When 4200 comes up, the output 4204 comes up immediately, since M4200 is on. The gate of M4200 is bootstrapped by gate-drain and gate-source capacitance so that 4204 reaches the same potential as 4200. While the trigger pulse is up, a pulldown pulse occurs on node 4203, turning off M4200 and pulling the output down.

Figure 68 shows the simple G6 generator. A pullup pulse and a pulldown pulse are required. The output is designed to have a maximum voltage of $V_{DD} - V_T$.

The connections of the generators G1 - G6 used to produce the internal timing pulses is shown in Figure 69. The approximate capacitive load of each

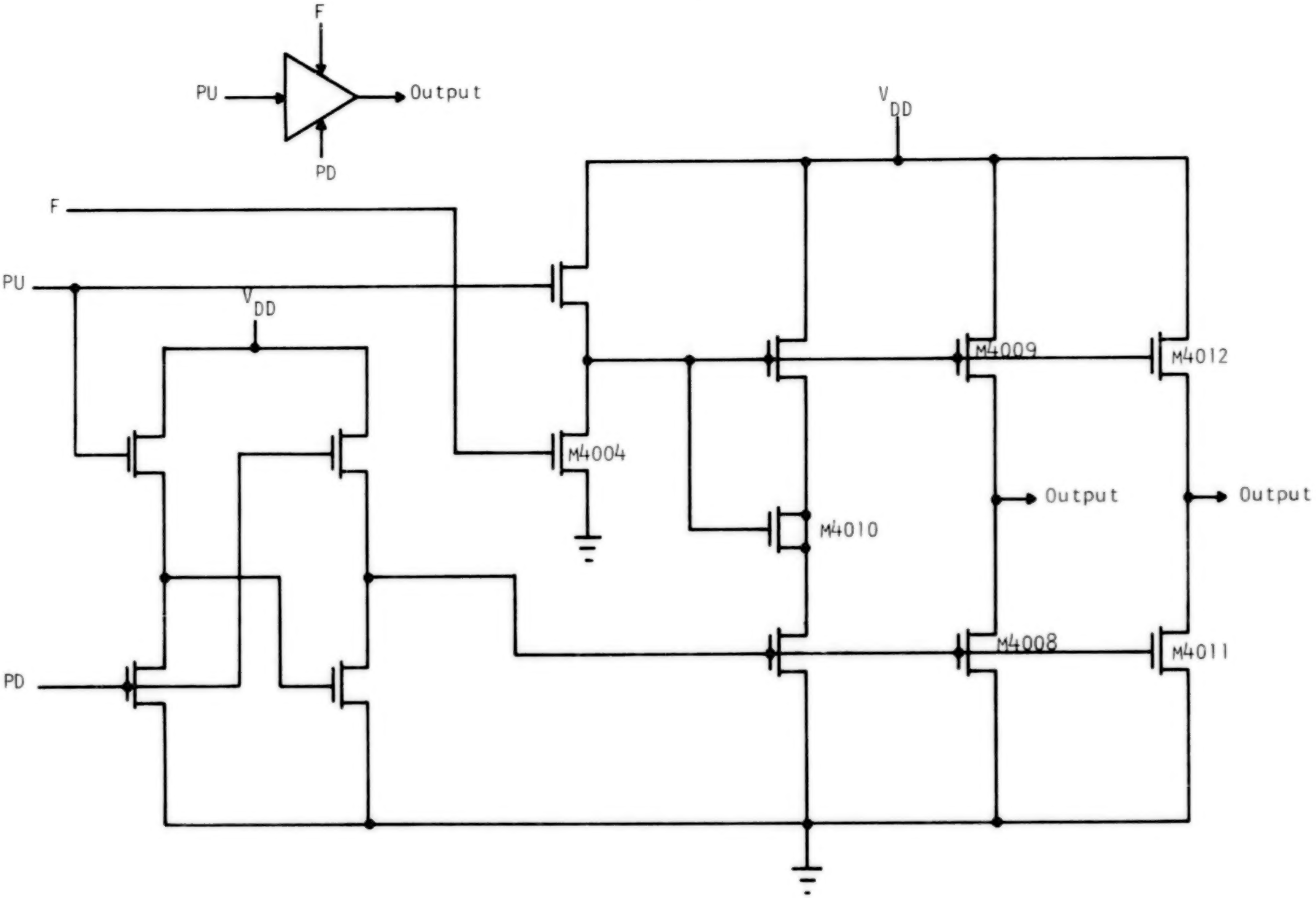

F
PU
Output
PD
V DD
F
PU
V DD
PD
M4004
M4009
M4012
M4010
Output
Output
M4008
M4011

Figure 64.- CCD $\phi_2^{\pm}$ Clock Pulse Generator.

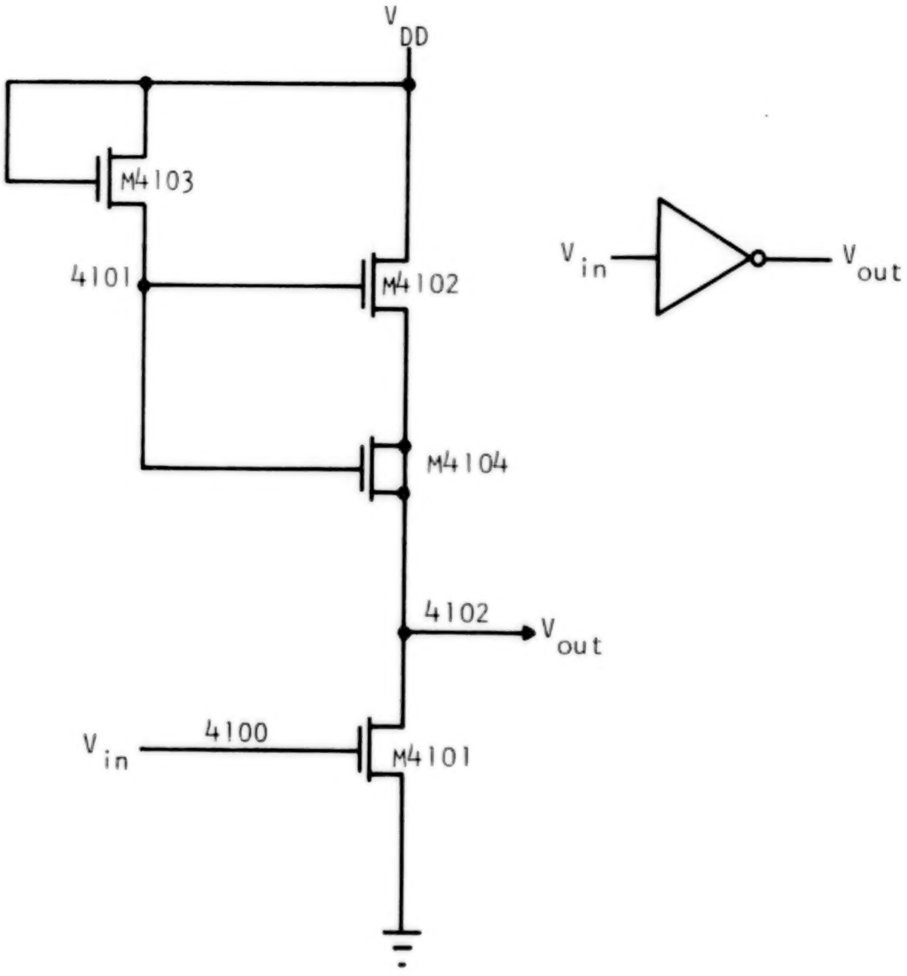

V_{DD}
M4103
4101
M4102
M4104
4102
V_{out}
V_{in}
4100
M4101
V_{in}
V_{out}

Figure 65.- G3 Inverter.

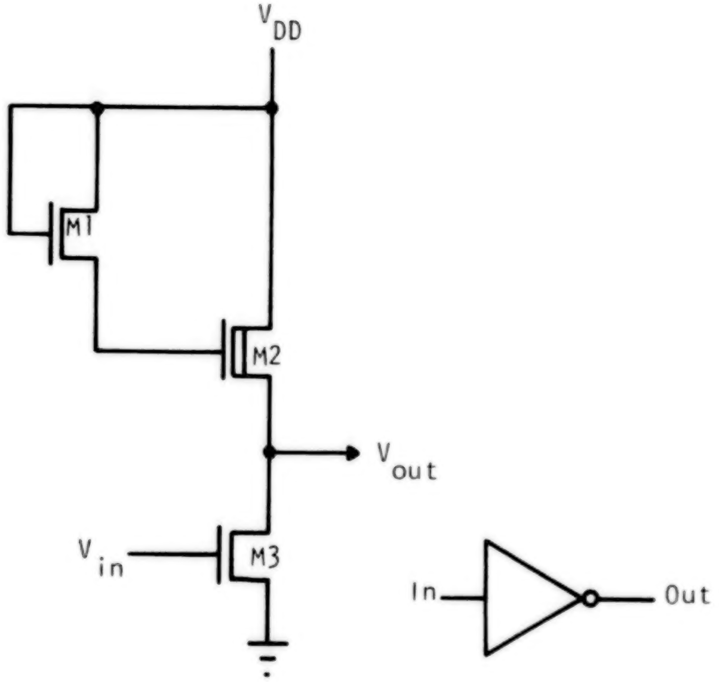

V_{DD}
M1
M2
V_{out}
V_{in}
M3
In
Out

Figure 66.-G4 Inverter.

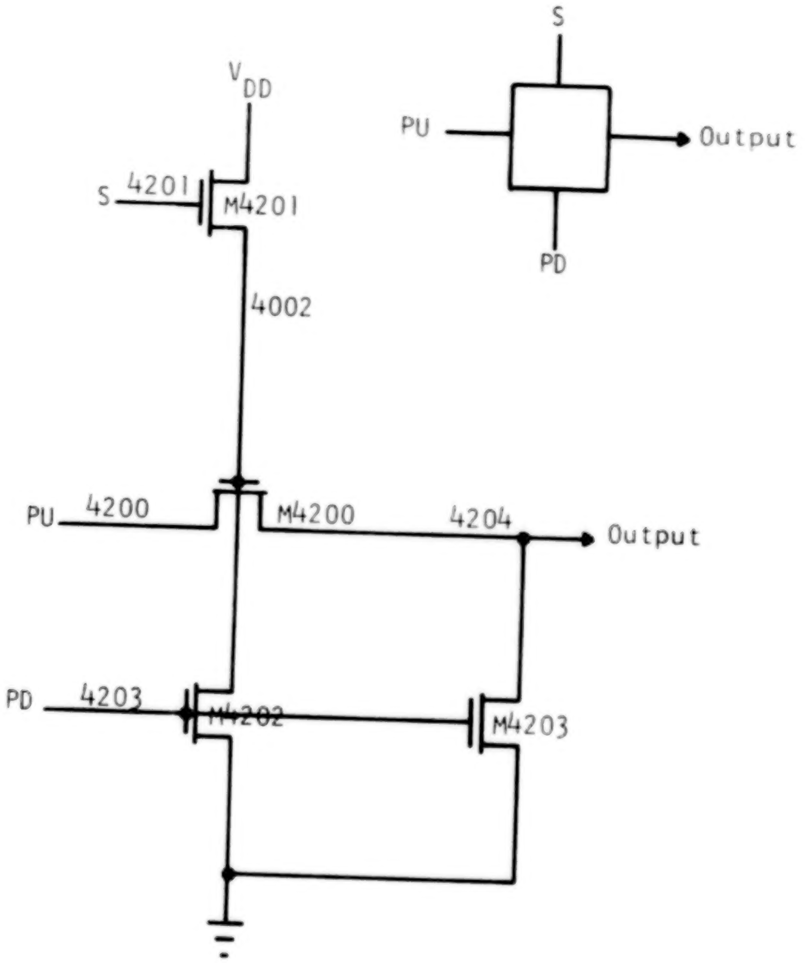

S
PU
Output
PD
V_{DD}
S
4201
M4201
4002
PU
4200
M4200
4204
Output
PD
4203
M4202
M4203

Figure 67.- G5 Generator.

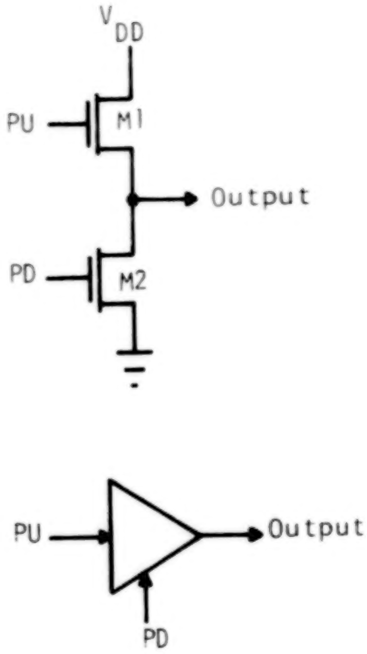

V_{DD}
PU
M1
Output
PD
M2
PU
Output
PD

Figure 68.-G6 Generator.

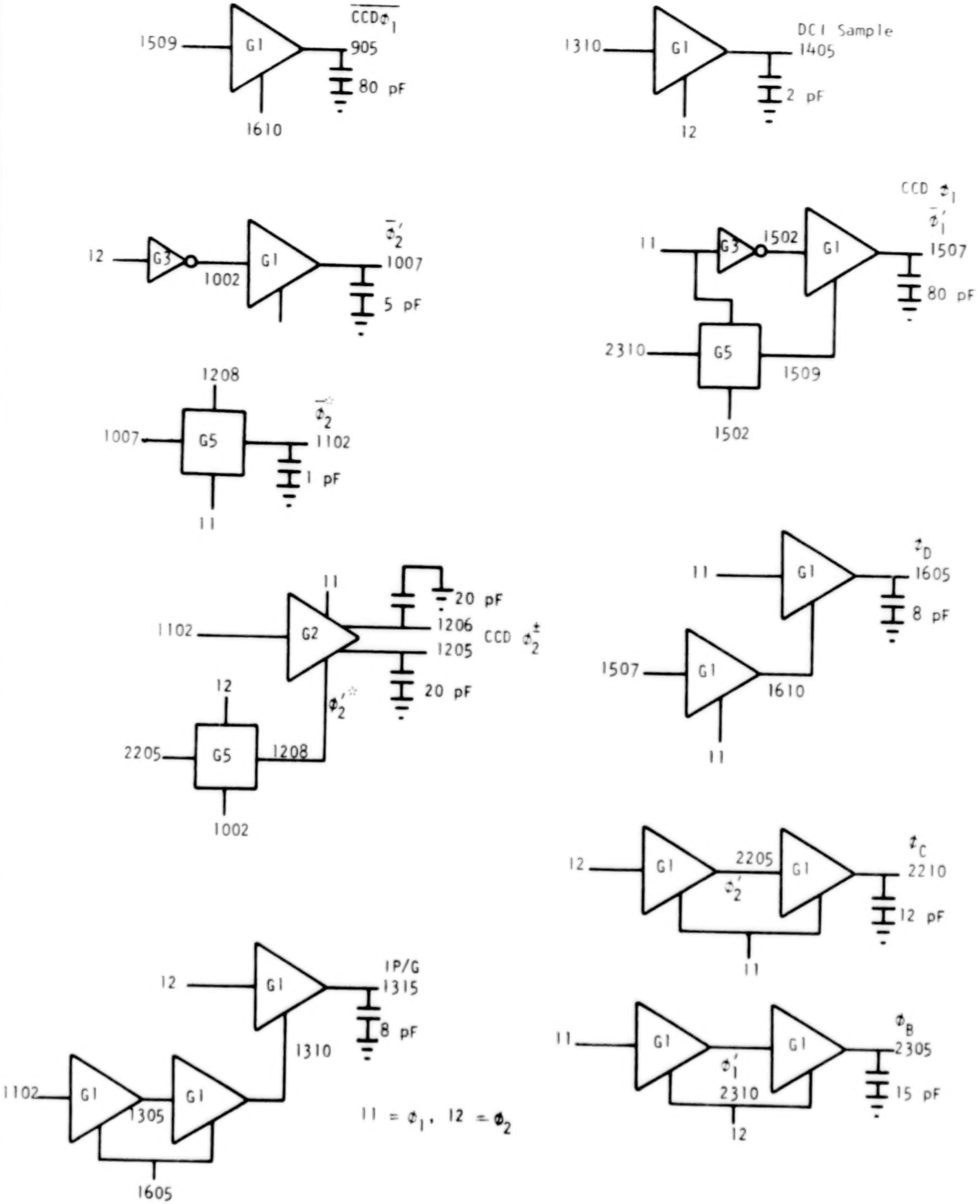
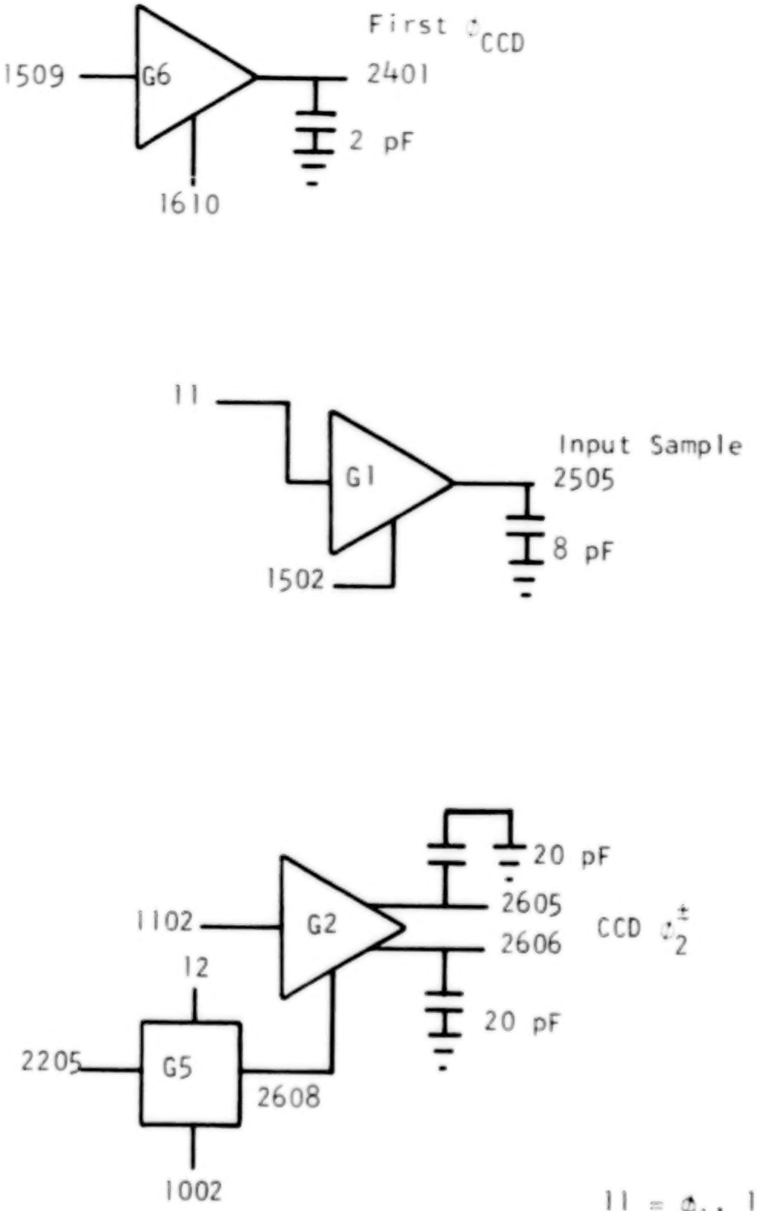

1509
G1
$\overline{CCD\phi_1}$
905
80 pF
1610
1310
G1
DCI Sample
1405
2 pF
12
12
G3
1002
G1
$\overline{\phi}_2'$
1007
5 pF
CCD ϕ_1
$\overline{\phi}_1'$
11
G3
1502
G1
1507
80 pF
2310
G5
1509
1502
1208
1007
G5
$\overline{\phi}_2^*$
1102
1 pF
11
11
1102
G2
20 pF
1206
CCD $\phi_2^{\pm}$
1205
20 pF
12
$\phi_2'^*$
2205
G5
1208
1002
ϕ_D
11
G1
1605
8 pF
1507
G1
1610
11
ϕ_C
12
G1
2205
ϕ_2'
G1
2210
12 pF
11
IP/G
12
G1
1315
8 pF
1310
1102
G1
1305
G1
1605
$11 = \phi_1, \; 12 = \phi_2$
ϕ_B
11
G1
ϕ_1'
2310
G1
2305
15 pF
12

Figure 69(a).- Connections of the Clock Generators Showing Capacitive Load of Each Driver.


First ϕ_{CCD}
1509
G6
2401
2 pF
1610
11
Input Sample
G1
2505
8 pF
1502
20 pF
1102
G2
2605
2606
CCD $\phi_2^{\pm}$
12
20 pF
2205
G5
2608
1002

$11 = \Phi_1$, $12 = \Phi_2$

Figure 69(b).- Connections of the Clock Generators Showing Capacitive Load of Each Driver.

driver as calculated from the bar layout is indicated. The node numbers correspond to the names given each set of generators and to the SPICE modeling performed. Many clock waveforms required series connections of G1 drivers to generate propagation delays critical to the chip timing. Figure 70 shows the resulting internal timing pulses as predicted by the computer simulation program, SPICE, for a clock period of 400 ns (2.5 MHz operation).

2. Experimental Results

Photographs of some of the actual clock waveforms are shown in Figure 71 through 73. These pulses were monitored on-chip with an external probe. Figure 71 shows the leading edge of ϕ_B and its pullup pulse ϕ_1. The ϕ_B leading edge is delayed from the ϕ_1 leading edge through two G1 drivers, as seen in Figure 69(a). The actual delay as seen in Figure 71(a) is about 60 ns. The risetime is 20 ns. The delay predicted by computer simulation was 55 ns, and the predicted risetime was 20 ns, as shown in Figure 70. Figure 71(b) shows the trailing edge of ϕ_B and its pulldown pulse ϕ_2. No delay is added to the ϕ_B trailing edge. The actual trailing edge delay is 30 ns, and the fall time is 15 ns. The predicted delay was 10 ns, and the predicted fall time was 15 ns, as shown in Figure 70. These results show close agreement between the computer simulations and the actual generator outputs. The ϕ_B and ϕ_C waveforms were designed to be complementary and nonoverlapping. Figure 72 illustrates the success of the design of these clocks. ϕ_C is generated using the same dual G1 driver configuration as ϕ_B with the pullup and pulldown pulses interchanged. Note that ϕ_B and ϕ_C are never high at the same time, and their leading and trailing edges do not overlap each other. Figure 72 may be compared to the computer-simulated timing of Figure 70.

A photograph of two of the larger clock generators (CCD $\phi_2^{\pm}$) is shown in Figure 73. These are G2 drivers as in Figure 64. It measures 1.75 x 0.4 mm^2 (69 x 16 mil^2).

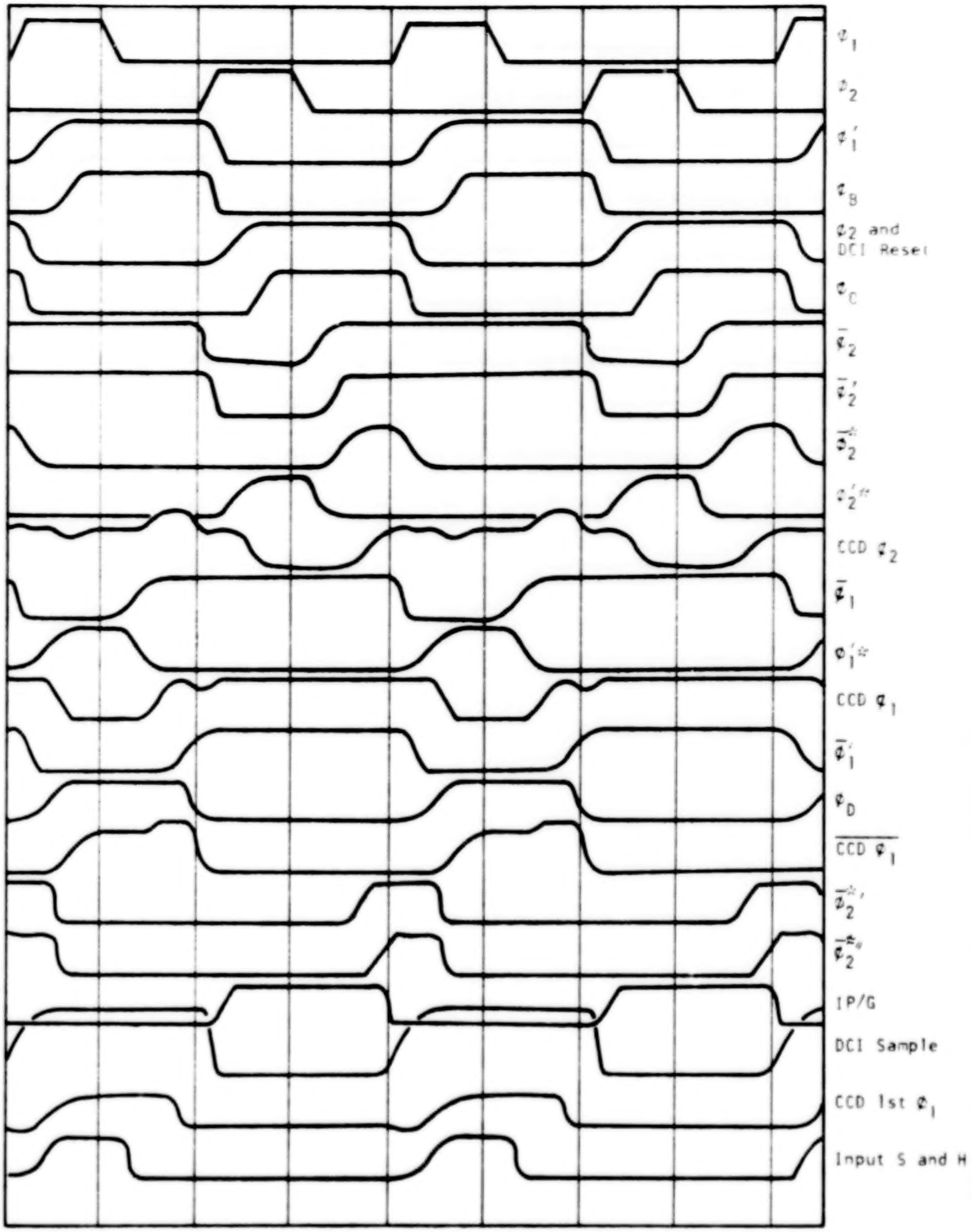

ϕ_1
ϕ_2
ϕ_1'
ϕ_B
ϕ_2 and DCI Reset
ϕ_C
$\bar{\phi}_2$
$\bar{\phi}_2'$
$\bar{\phi}_2^{*}$
$\phi_2'^{\#}$
CCD ϕ_2
$\bar{\phi}_1$
$\phi_1'^{*}$
CCD ϕ_1
$\bar{\phi}_1'$
ϕ_D
$\overline{\text{CCD } \phi_1}$
$\bar{\phi}_2^{*\prime}$
$\bar{\phi}_2^{*\prime\prime}$
IP/G
DCI Sample
CCD 1st ϕ_1
Input S and H

Figure 70.-System Timing.

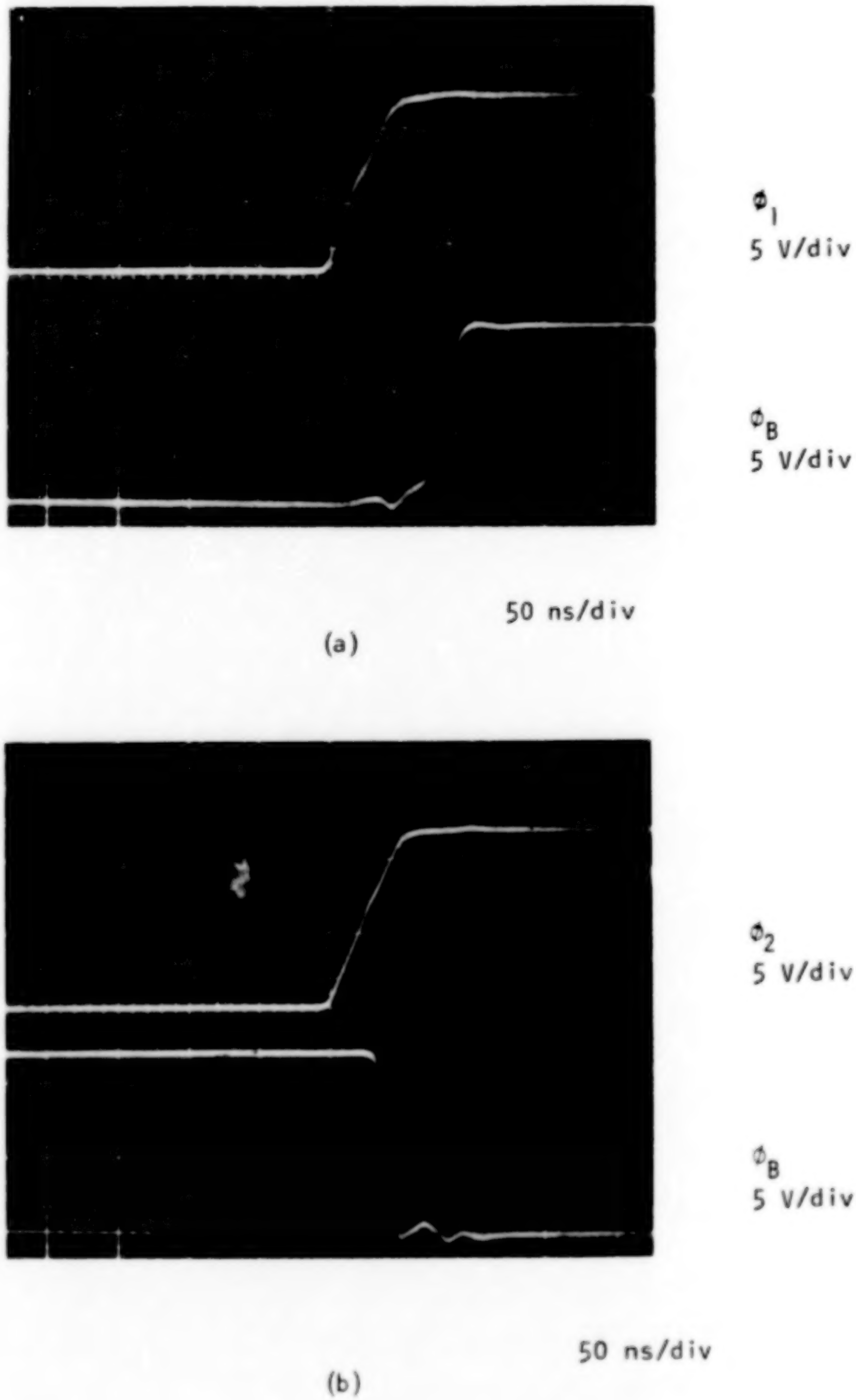


Figure 71.-Clock Circuit Performance.

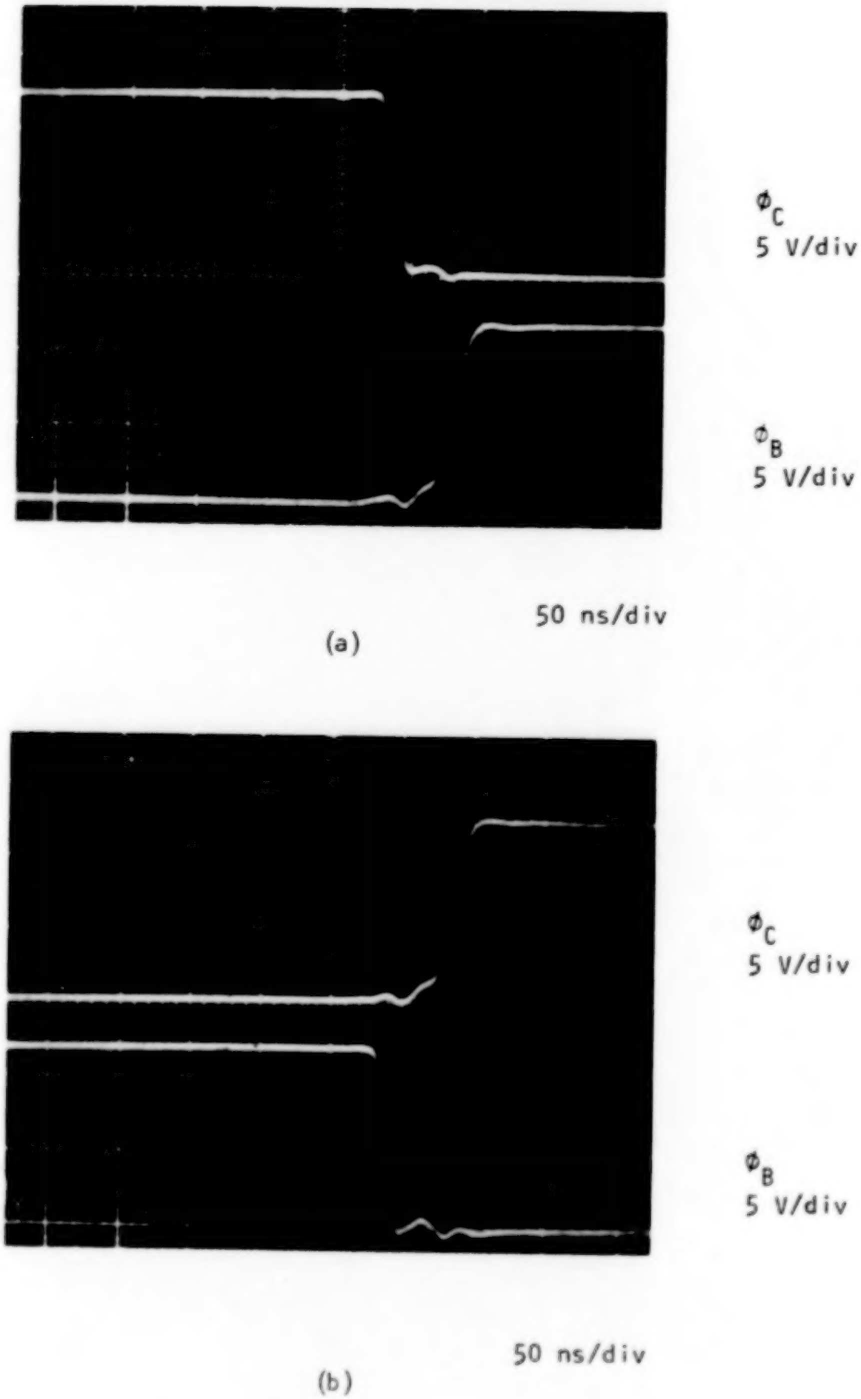


Figure 72.-Relationship of ϕ_B and ϕ_C.

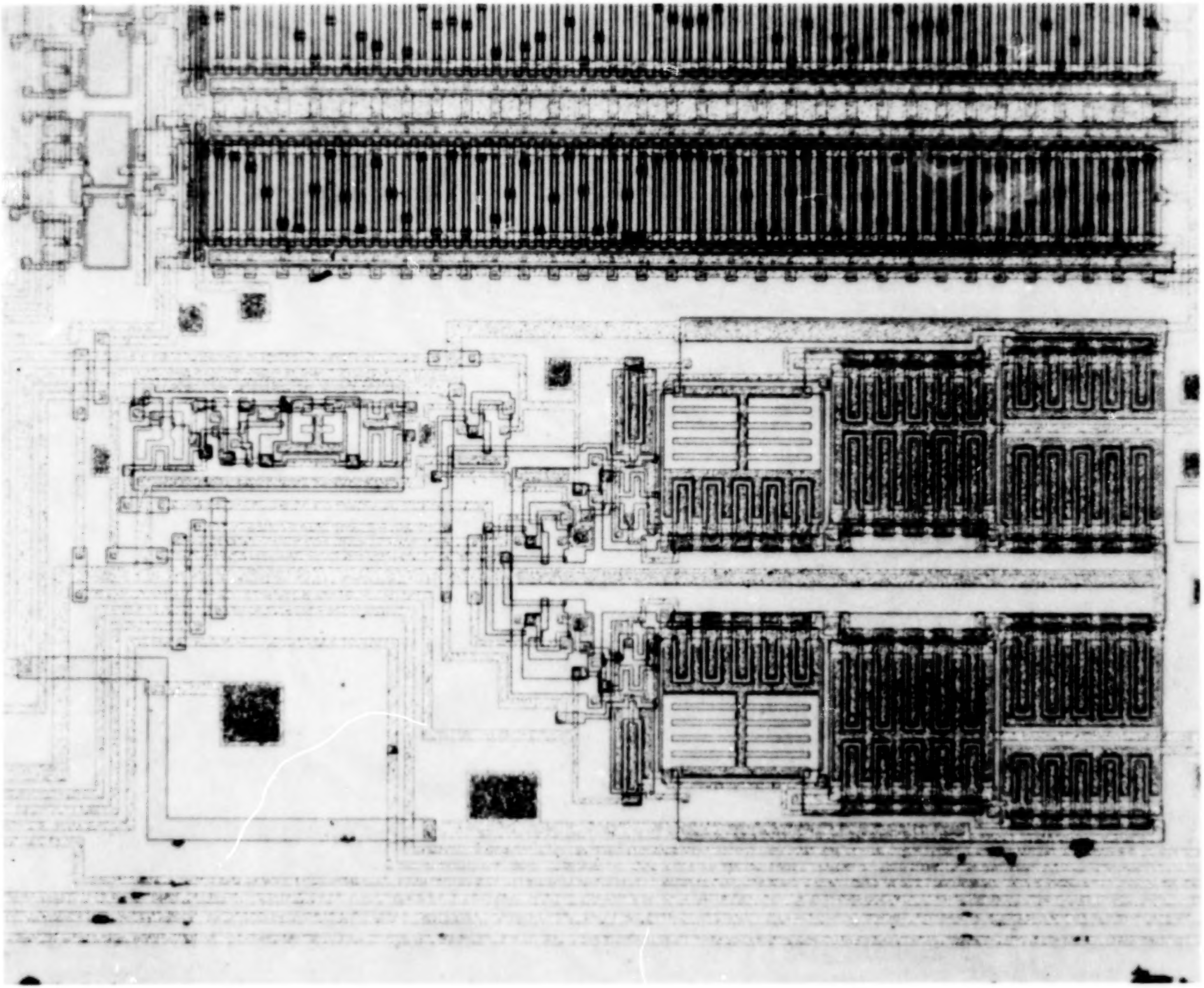


Figure 73.- Photograph of CCD ϕ_2 Clock Driver.

G. Experimental Results

Evaluation of the CZT IC has been confined to obtaining power density spectra of real inputs using the system shown in Figure 74. This system requires only two MOS level clocks, voltage bias for the various circuits, and the squaring function. Figures 75 through 79 are photographs showing the operation of the CZT IC. Figure 75 shows the operation of the IC with 10 kHz clocks and no postmultiplication. The upper photograph shows the response of the MDACs to a dc input and the internal ROM. The bottom photograph shows the response of the IC to a 1.8 kHz sinusoid. The output shows the envelope of the real and imaginary outputs, since the input is not synchronized to the chip clocks. Similar operation of the IC is shown in Figure 76 with 1 MHz clocks. The input signal is a 440 kHz sinusoid with a dc offset. Figure 76 also illustrates a problem with the tapweights of the filters. The CCD tapweights were erroneously shifted one bit, causing the 32nd bit to appear as the first bit, while the first bit shifts to the second bit, and so on. This will affect only spectral power density analysis in that the output sequence is rotated. It will also affect function implementations requiring postmultiplications. To perform postmultiplications, a second chip will be required whose timing is delayed by one clock period. This error can easily be corrected with photomask changes.

Figure 77 shows the power density spectra for three different sinusoidal inputs with a dc offset. The output is observed to be delayed as the input frequency increases from 625 Hz to 4.0 kHz. Similar operation is shown in Figure 81 with 1 MHz clocks and the input varying from 125 kHz to 375 kHz. The apparent sidelobes are caused by the limited bandwidth and inaccuracies of the squaring devices. The response of the CCD CZT IC to a 312.5 Hz and a 625 Hz square wave input is shown in Figure 79. The output can be seen to decrease as $1/n^2$ (where n is the harmonic index).

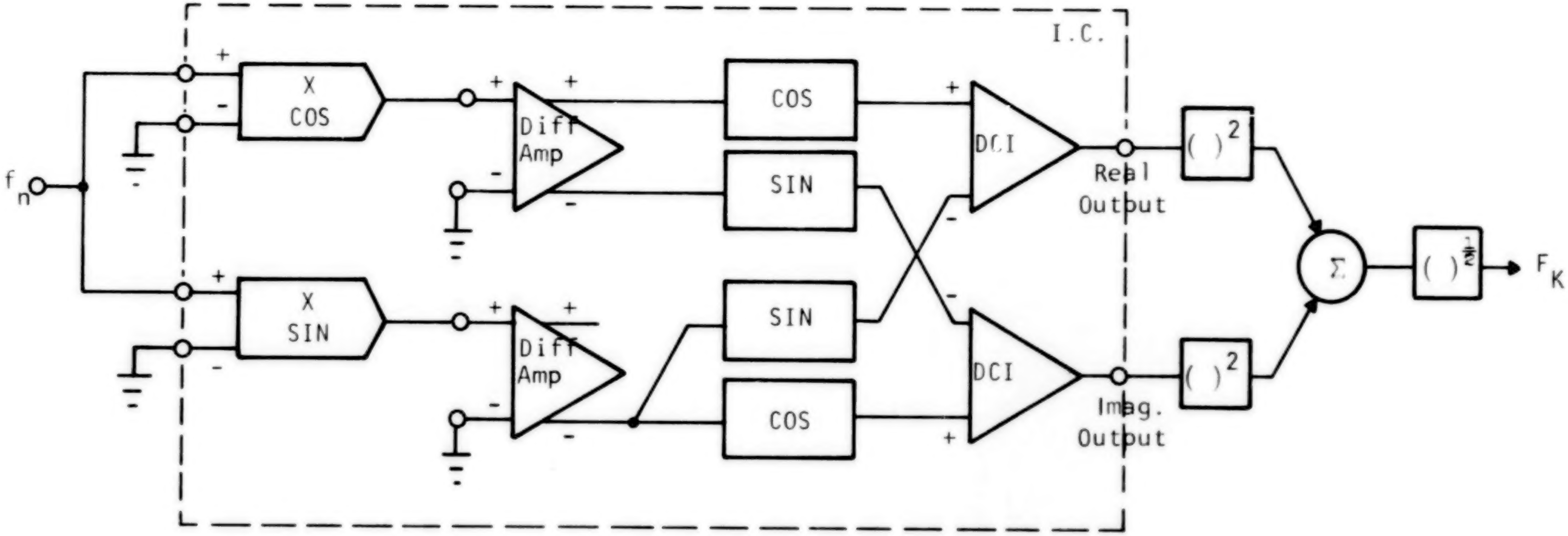
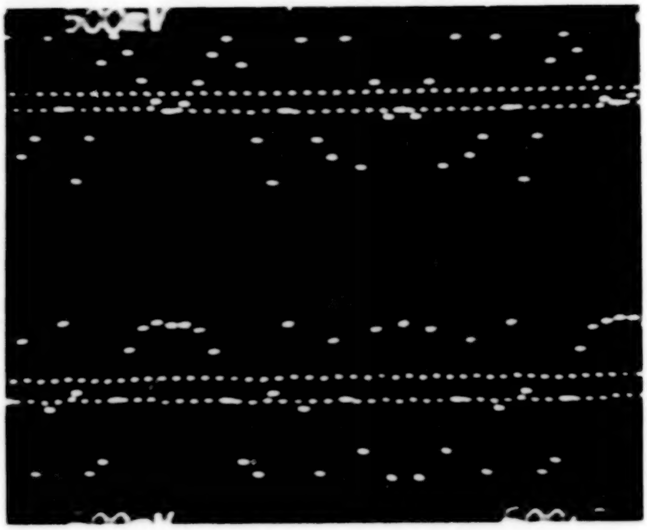
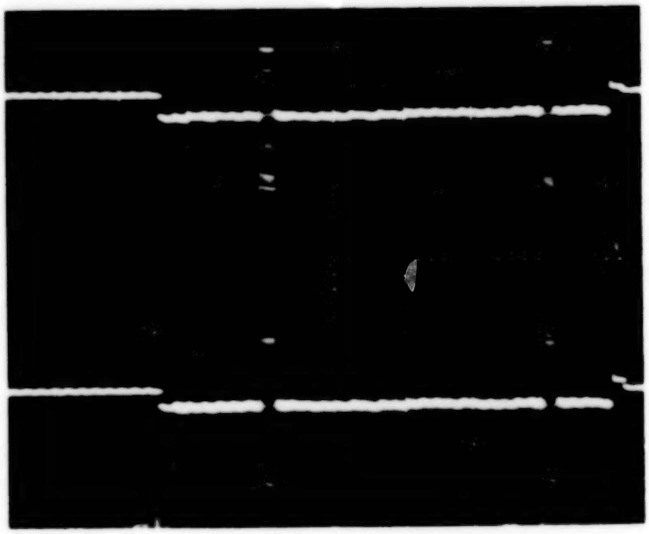

I.C.
f_n
+
-
X COS
X SIN
+
-
Diff Amp
Diff Amp
COS
SIN
SIN
COS
DCI
DCI
Real Output
Imag. Output
( )^2
( )^2
Σ
( )^½
F_K

Figure 74.-A System for Obtaining Power Density Spectrum of a Real Input Using One CZT IC (50% Input/Output Duty Cycle).

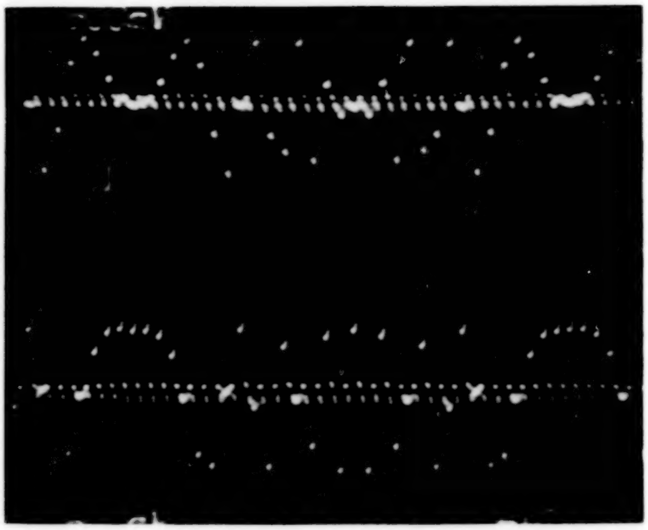


(a) Response of MDACs to dc Input and Internal ROM

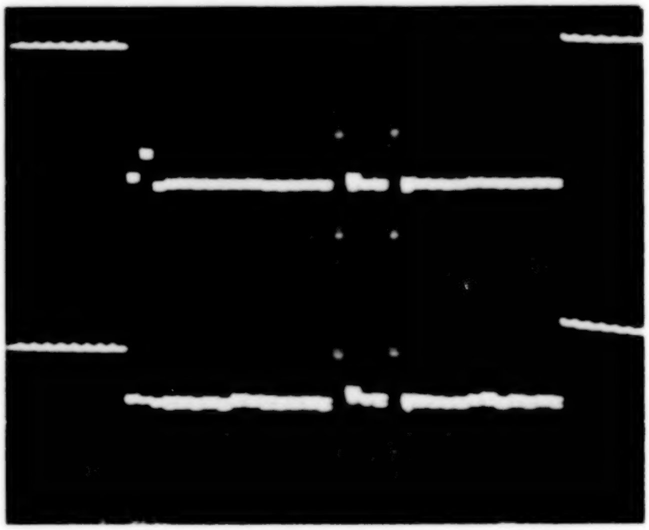


(b) Response of IC to 1.8 kHz Sinusoid

Figure 75.-Operation of CCD CZT IC with 10 kHz Clocks.



(a) Response of MDACs to dc Input and Internal ROM.



(b) Response of IC to 440 kHz Sinusoid.

Figure 76.-Operation of CCD CZT IC with 1 MHz clocks.

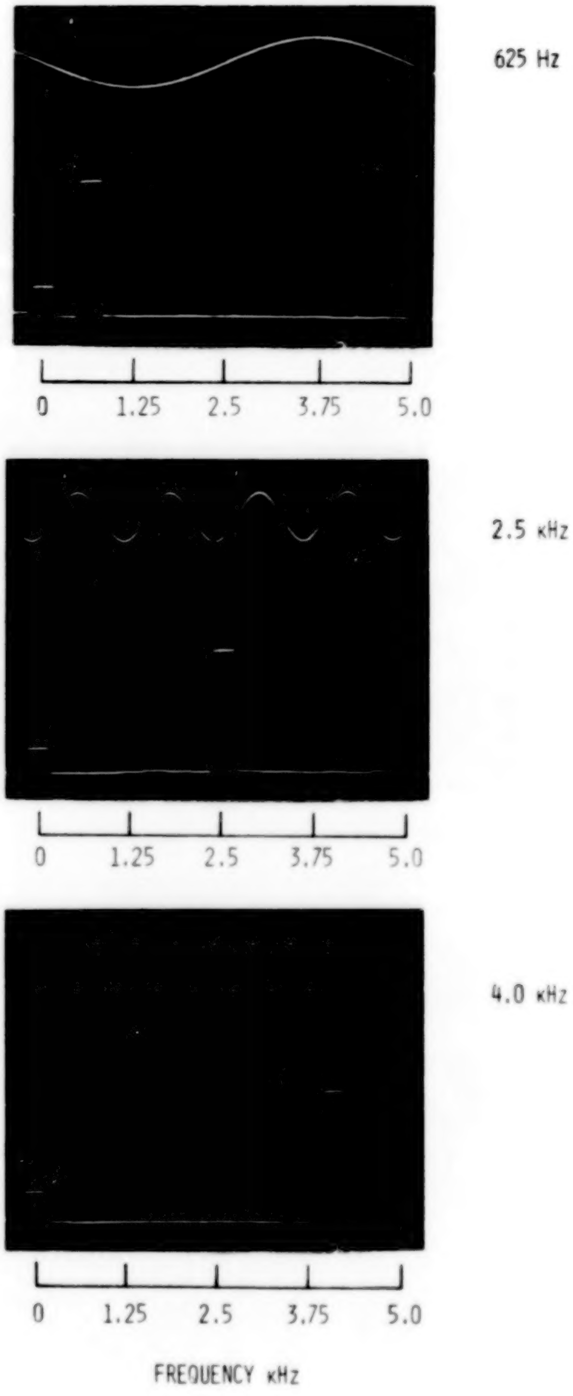


Figure 77.- Power Density Spectra for Three Sine Waves Obtained Using the 32-Point CCD CZT at a 10 kHz Sample Rate.

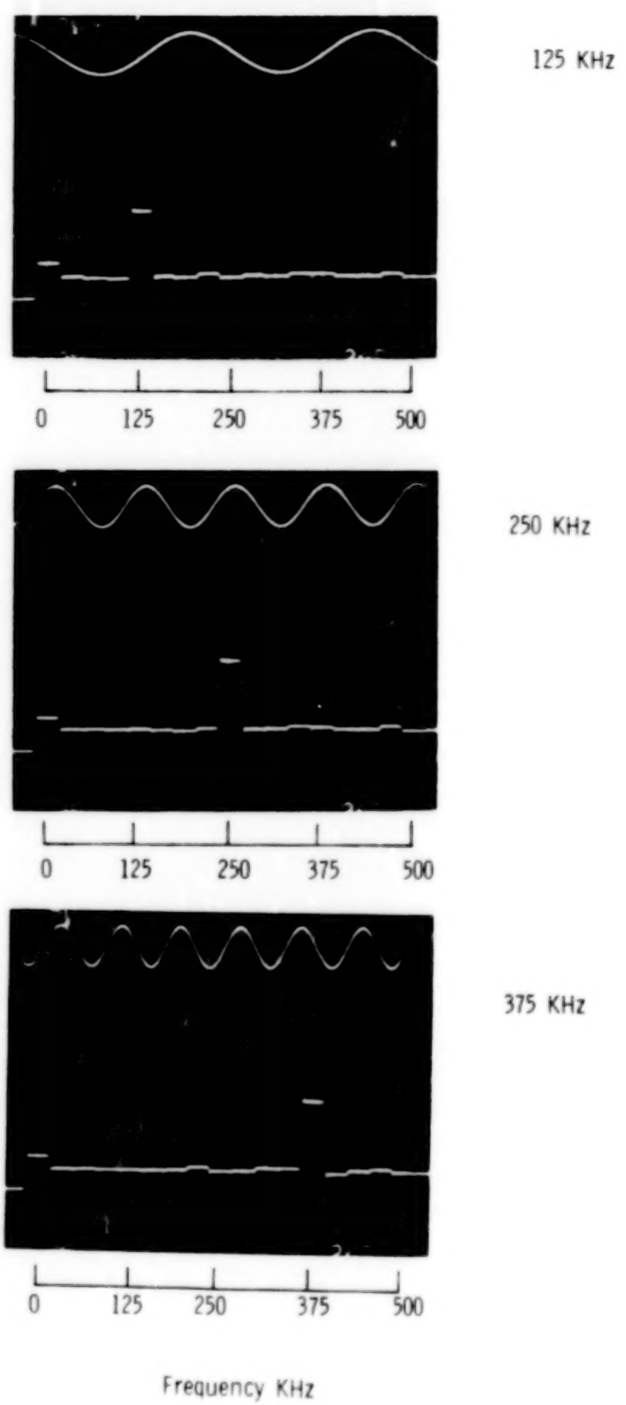
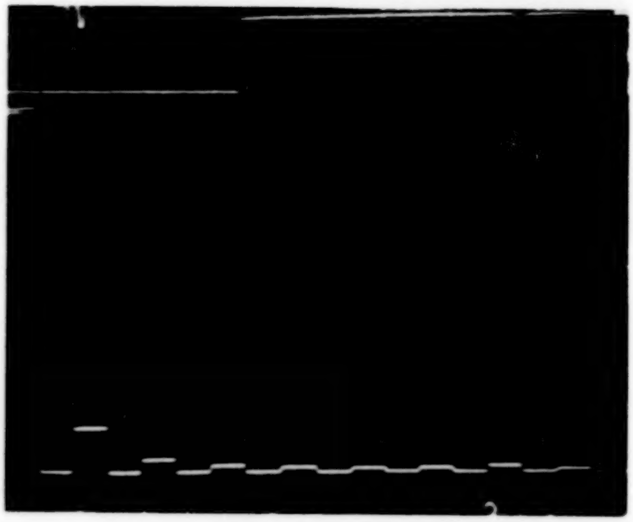


Figure 78.-Power Density Spectra for Three Sine Waves Obtained Using the 32 Point CCD CZT at 1 MHz Sample Rate.



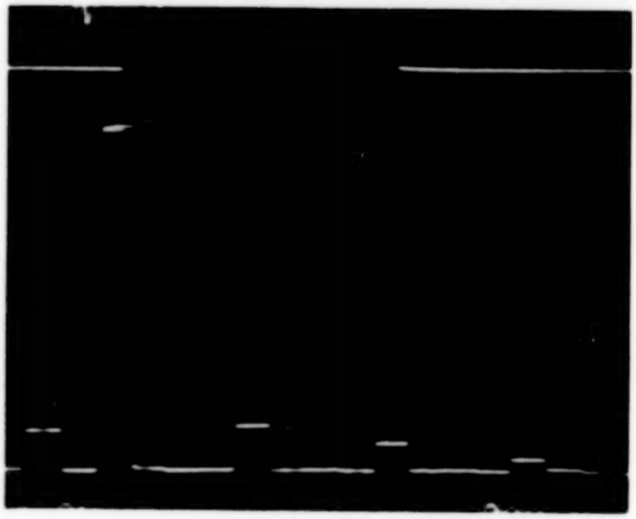


Figure 79.- Response of CCD CZT IC to Square-Wave Inputs (10 kHz Clock Frequency)

H. Applications

The most straightforward application of the 32-point CCD CZT IC is to obtain power density spectra using the block diagram of Figure 74.

With a few external components, a complex input/output CZT can be performed with one chip as shown in Figure 80. The external components are necessary to disable the inputs when a postmultiply operation is needed for the true CZT. Because of this blanking, the system in Figure 80 has only a 50% input/output duty cycle. To obtain a 100% input/output duty cycle CZT, two chips are needed as shown in Figure 81. This configuration does not require the external circuitry of Figure 80.

The realization of a 16-point correlator using two CZT ICs is shown in Figure 82. This correlator convolves the real input signal with an impulse response h(t). True correlation is obtained, since the pulse T_1 can blank the CCD input when required.

Another application (not shown) is the realization of a 16-point programmable transversal filter. This realization would require eight CZT ICs arranged as four correlators of the type shown in Figure 82. T_1 and T_2 will provide synchronization between the chips. These correlators would have the inputs tied together and their outputs summed.

These are only a few of the many applications the general-purpose CZT IC can perform, but they demonstrate its tremendous computational power.

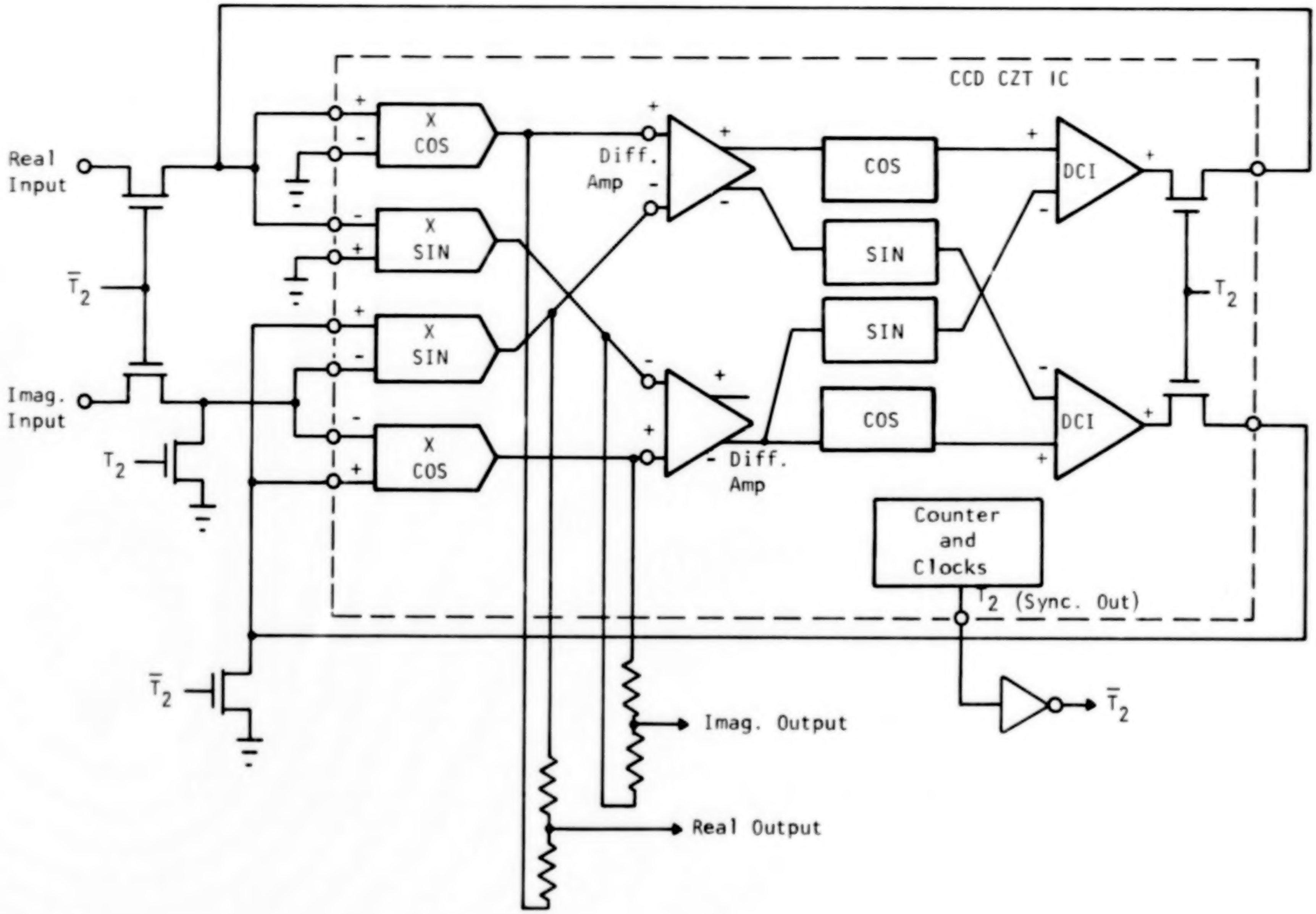

CCD CZT IC
Real Input
Imag. Input
$\overline{T}_2$
T_2
X COS
X SIN
X SIN
X COS
Diff. Amp
Diff. Amp
COS
SIN
SIN
COS
DCI
DCI
Counter and Clocks
T_2 (Sync. Out)
$\overline{T}_2$
Imag. Output
Real Output
+
-

Figure 80.-Realization of Complex I/O CZT with One Chip (50% Duty Cycle).

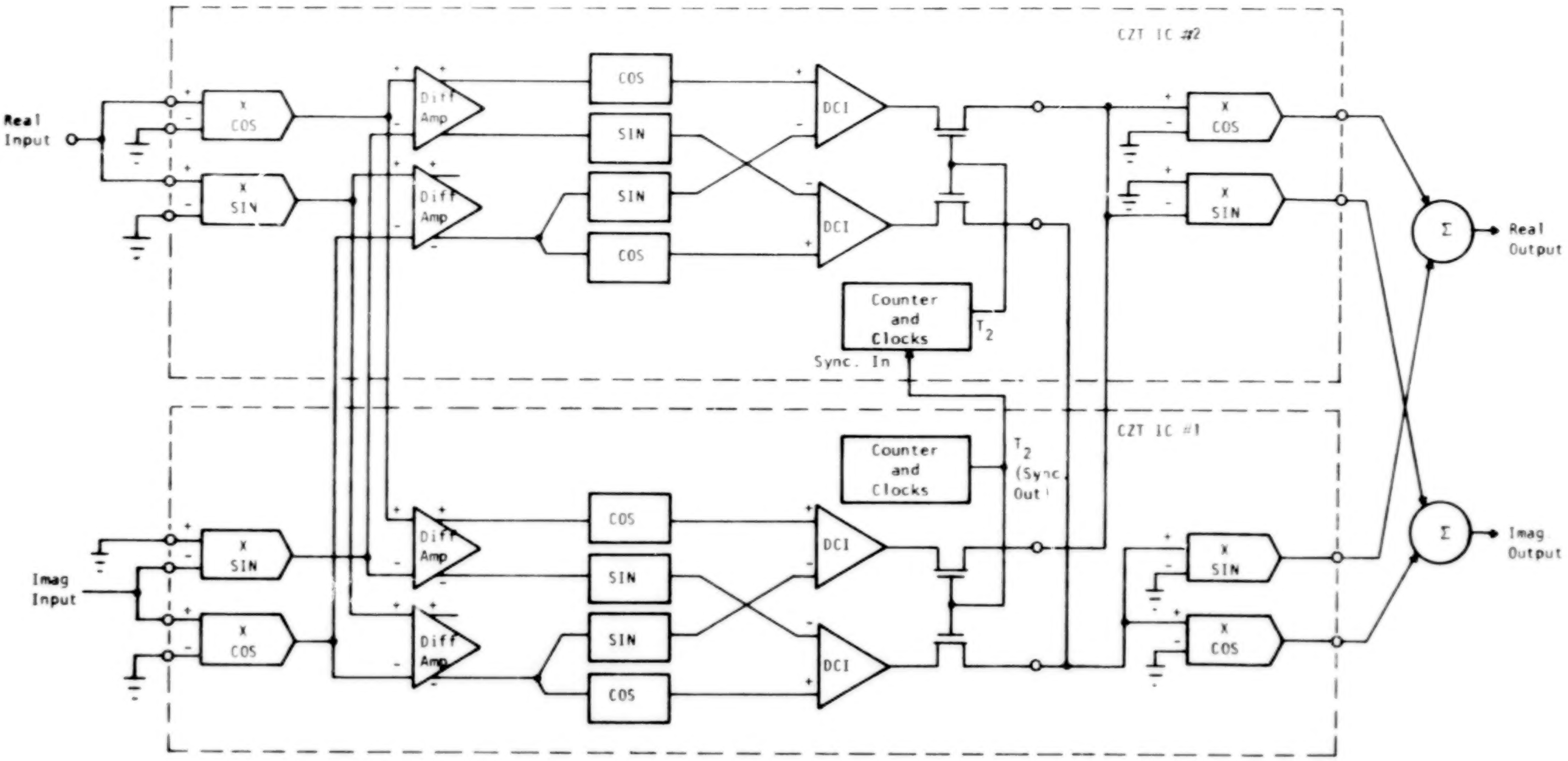

CZT IC #2
Real Input
X COS
X SIN
Diff Amp
Diff Amp
COS
SIN
SIN
COS
DCI
DCI
X COS
X SIN
Σ
Real Output
Counter and Clocks
T_2
Sync. In
CZT IC #1
Counter and Clocks
T_2 (Sync. Out)
Imag Input
X SIN
X COS
Diff Amp
Diff Amp
COS
SIN
SIN
COS
DCI
DCI
X SIN
X COS
Σ
Imag. Output

Figure 81.- Realization of Complex I/O CZT Using Two CZT ICs (100% I/O Duty Cycle).

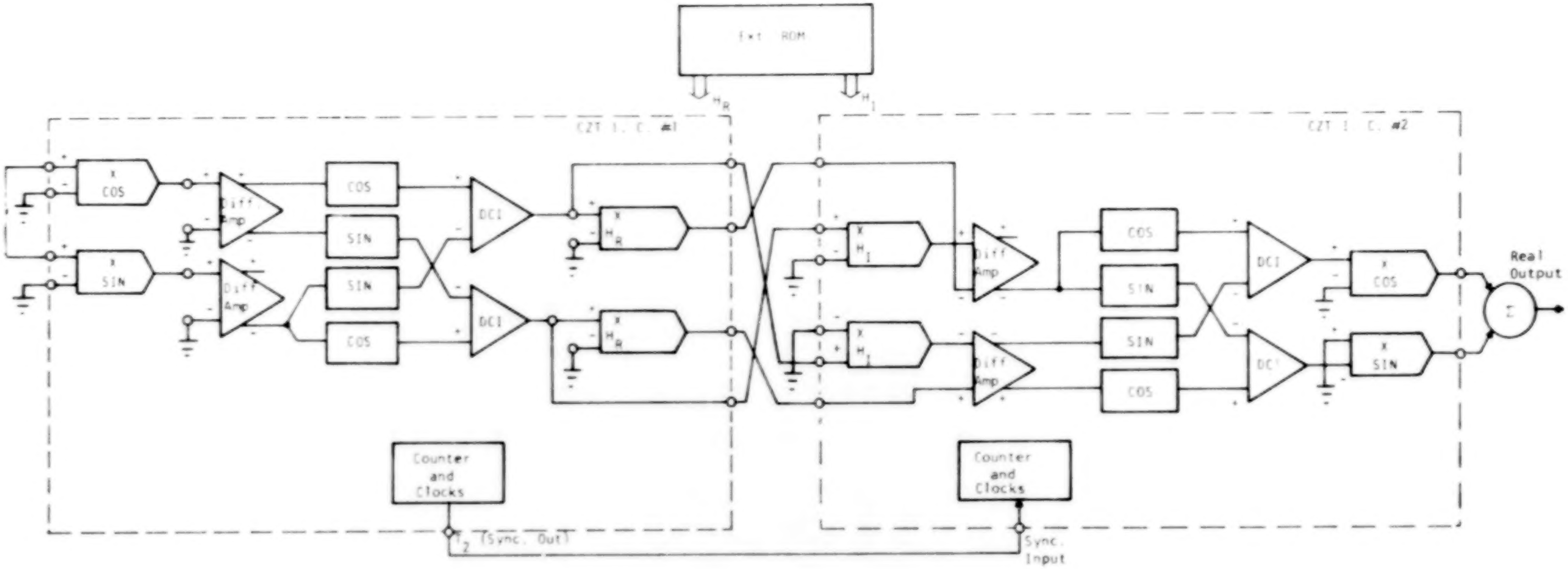

Ext. ROM
H_R
H_I
CZT I. C. #1
CZT I. C. #2
X COS
X SIN
Diff. Amp
Diff Amp
COS
SIN
SIN
COS
DCI
DCI
X H_R
X H_R
X H_I
X H_I
Diff Amp
Diff Amp
COS
SIN
SIN
COS
DCI
DCI
X COS
X SIN
Σ
Real Output
Counter and Clocks
Counter and Clocks
T_2 (Sync. Out)
Sync. Input

Figure 82.- Realization of Correlator Using Two CZT ICs (Real 25% Duty Cycle Input, Real 50% Duty Cycle Output).

SECTION III

64-POINT CCD ANALOG/ANALOG CORRELATOR

A. Design

The convolver is organized according to the block diagram of Figure 83. Two 64-stage CCDs shift charge in opposite directions. At each stage non-destructive outputs are obtained using floating gate amplifiers. Signals are buffered, and corresponding outputs from each stage are passed to analog multipliers. The outputs of the multipliers are summed to complete the function. Feedback linearization from the first buffer output is provided to remove circuit nonlinearities.

Parallel outputs are obtained using floating gates, as in Figure 84. A floating first poly electrode is placed underneath the phase-two clock. The floating gate is capacitively coupled to the CCD channel potential. The output voltage is attenuated approximately 50% due to parasitic capacitances, mostly capacitance to the phase-two clock. The floating gates are periodically reset through small series FETs to a reference.

The analog multiplier is shown in Figure 85, together with the required buffers. Each buffer is biased by a FET current source. The multiplier itself is a two-transistor circuit, which eliminates the effects of drain resistance nonlinearity, as shown below. The current in each of the multiplier FETs as a function of the terminal voltages is:

$$\begin{aligned} I_{d2} &= B(V_{gs2} - V_t - \tfrac{1}{2}V_{ds})V_{ds} + f(V_{ds}) \\ I_{d1} &= B(V_{gs1} - V_t - \tfrac{1}{2}V_{ds})V_{ds} + f(V_{ds}) \quad . \end{aligned} \tag{15}$$

where $f(V_{ds})$ is the next higher order approximation for the current, which takes into account the transistor threshold voltage variation with substrate voltage. It is only a function of V_d and V_s. Subtracting the two currents we obtain:

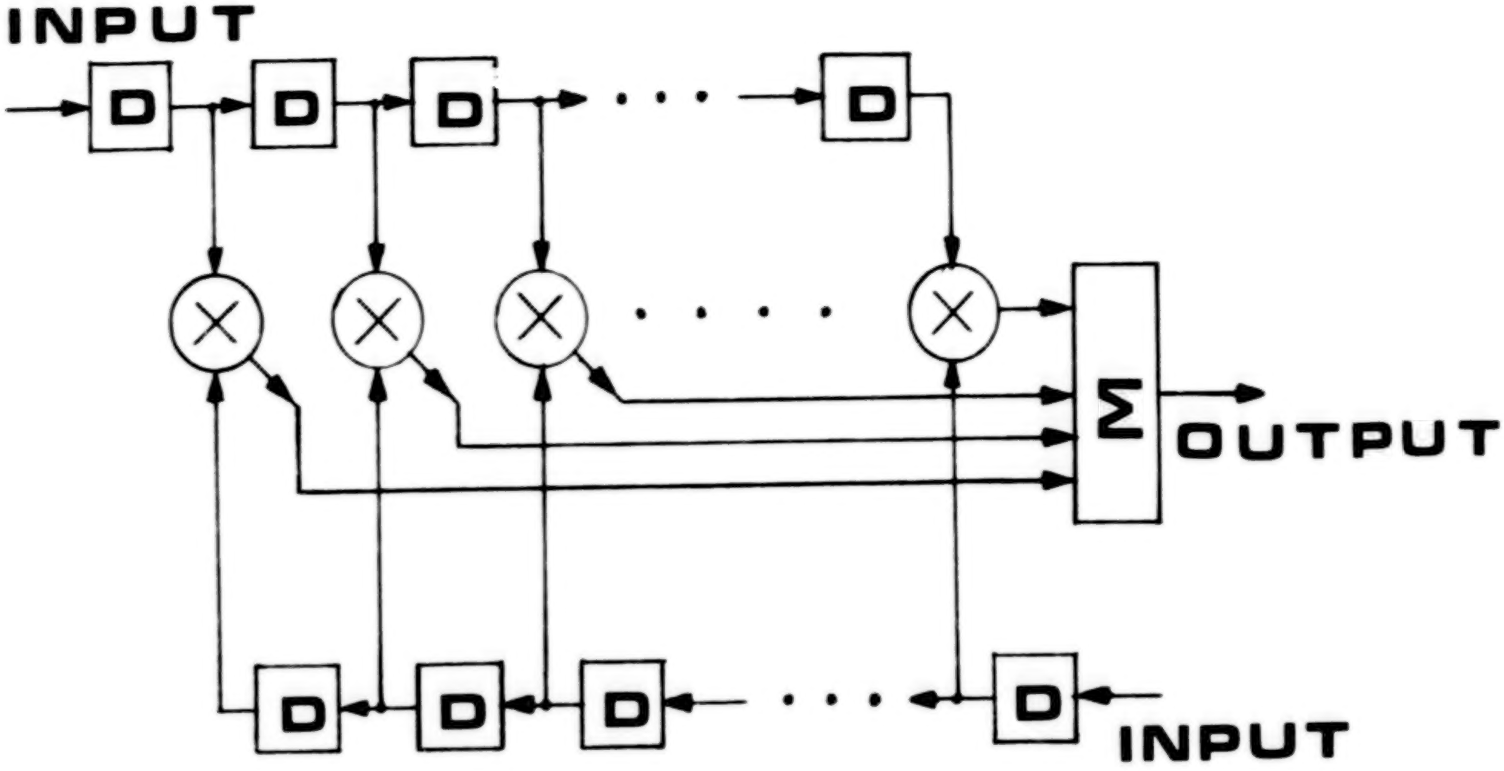

INPUT
D
D
D
D
Σ
OUTPUT
D
D
D
D
INPUT

Figure 83.–Analog Correlator Block Diagram.

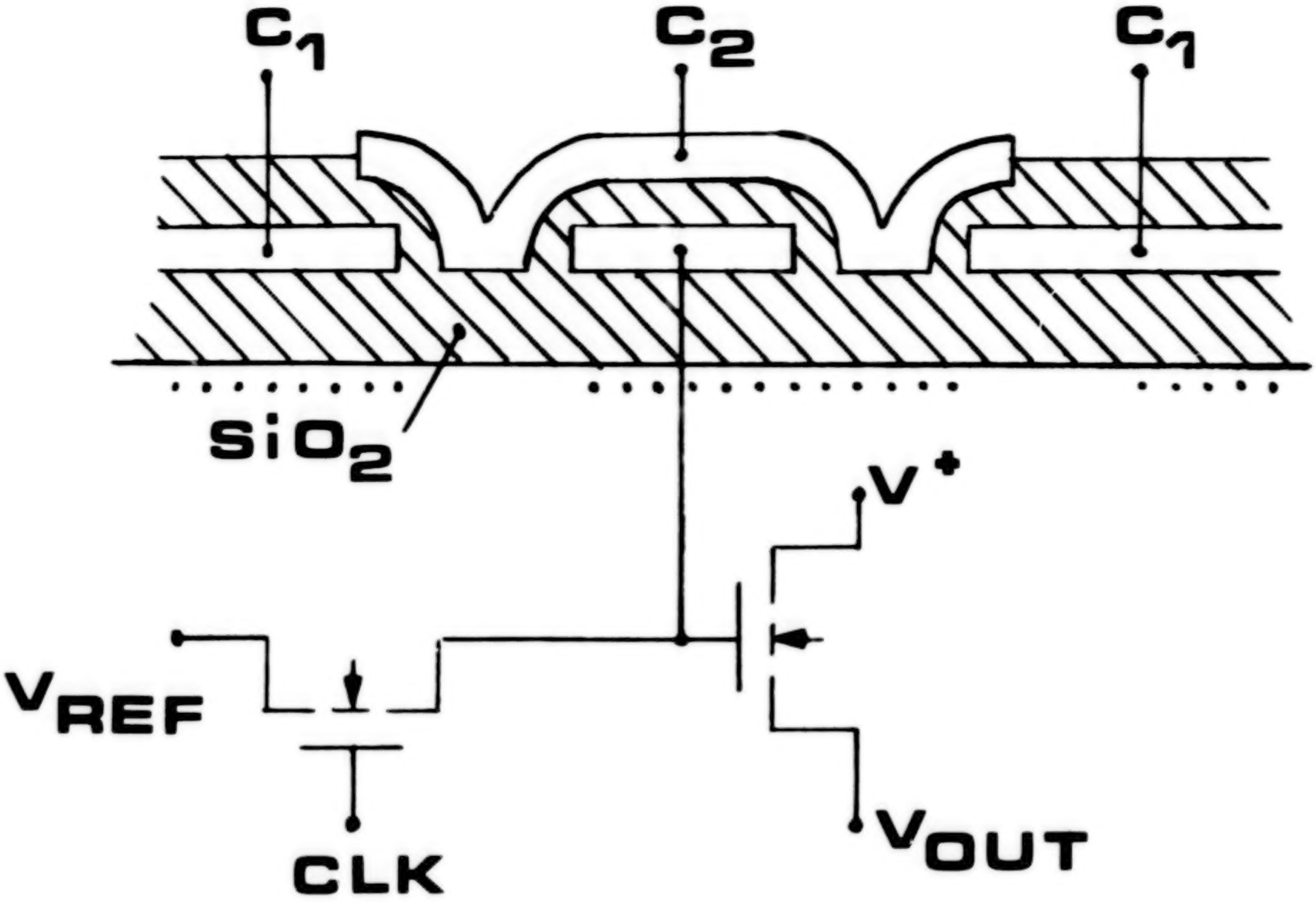

C1
C2
C1
SiO2
V+
VREF
CLK
VOUT

Figure 84.-Floating Gate Reset Technique.

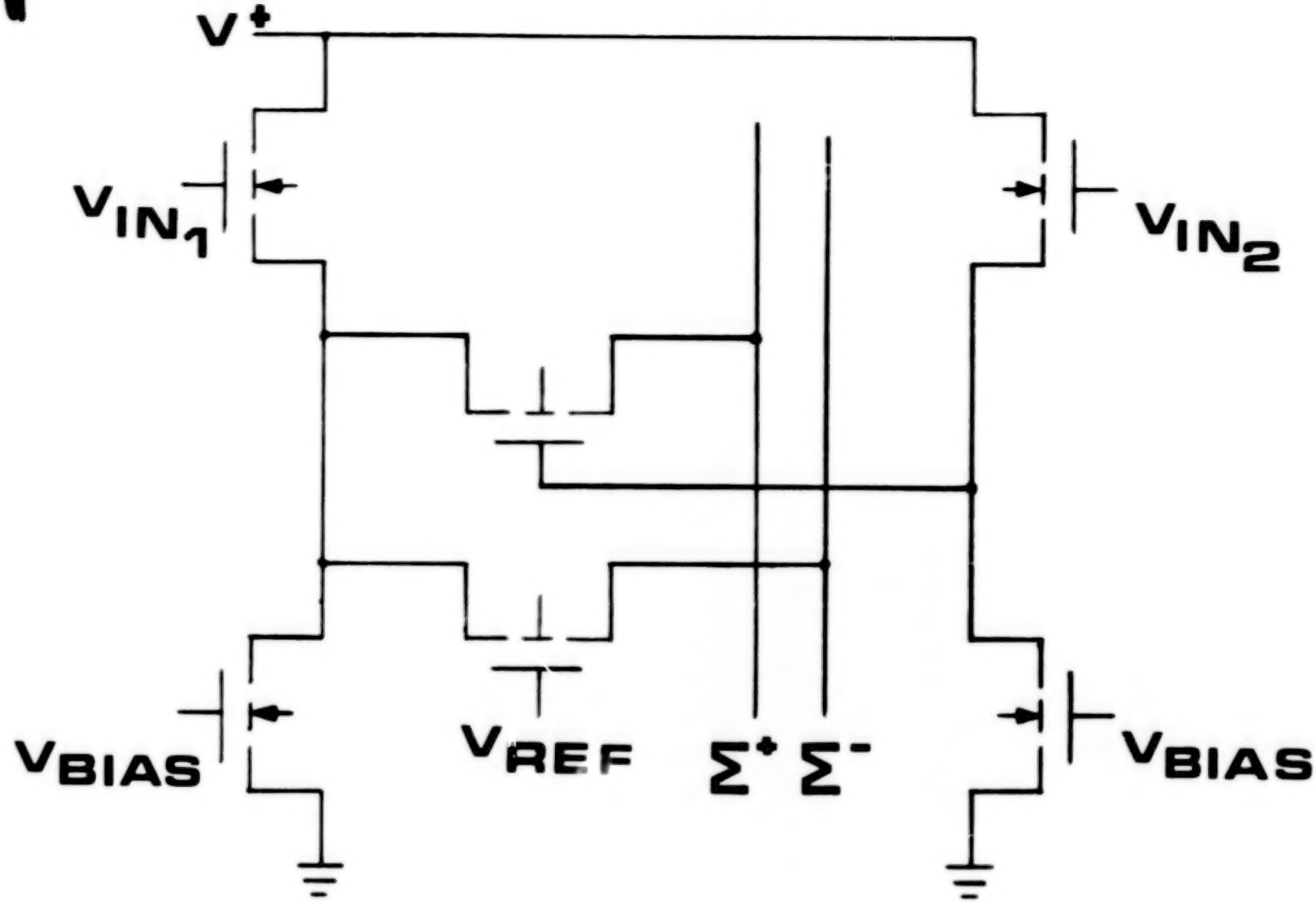

V^+
V_{IN_1}
V_{IN_2}
V_{BIAS}
V_{REF}
Σ^+
Σ^-
V_{BIAS}

Figure 85.-Analog Multiplier.

$$I_{d2} - I_{d1} = B(V_{gs2} - V_{gs1})\ V_{ds} \quad , \qquad (16)$$

since the drain and source voltages are identical for the two devices. Note that the drain nonlinearities, as well as the higher order terms, have cancelled. The residual nonlinearities that remain arise from variation in FET transconductance with gate voltage and from buffer output impedance.

A feedback linearization circuit has been incorporated into the input stage to control the dc voltage levels and eliminate nonlinearities in the CCD input to buffer output transfer function. It is shown in Figure 86. The input stage is identical to the other CCD stages and has its own floating gate output and buffer. Charge is input to the CCD stage through a FET, where the input signal is on the source (the input diode), and the feedback signal is on the gate (the feedback gate). As the charge fills up the well in the CCD input stage, the floating gate senses it, and the voltage level of the feedback gate drops until it is a threshold above the voltage on its source. Thus, the relative input and buffer output voltage levels depend only on the characteristics of the input FET, and not on all the other adjustments required to make the device operate, such as the floating gate reference voltage.

Note that the charge is metered into the input well in exactly the right amount to provide a linear output from the buffer, and the buffer nonlinearity caused by body effect and static loading becomes unimportant.

B. Performance Limitations in Design

1. Multiplier Nonlinearity

There are two main sources of multiplier nonlinearity. The first is due to the variation in FET transconductance with gate voltage. It comes from carrier velocity saturation effects to a small degree, but mostly from the variation in surface mobility as a function of surface concentration. That

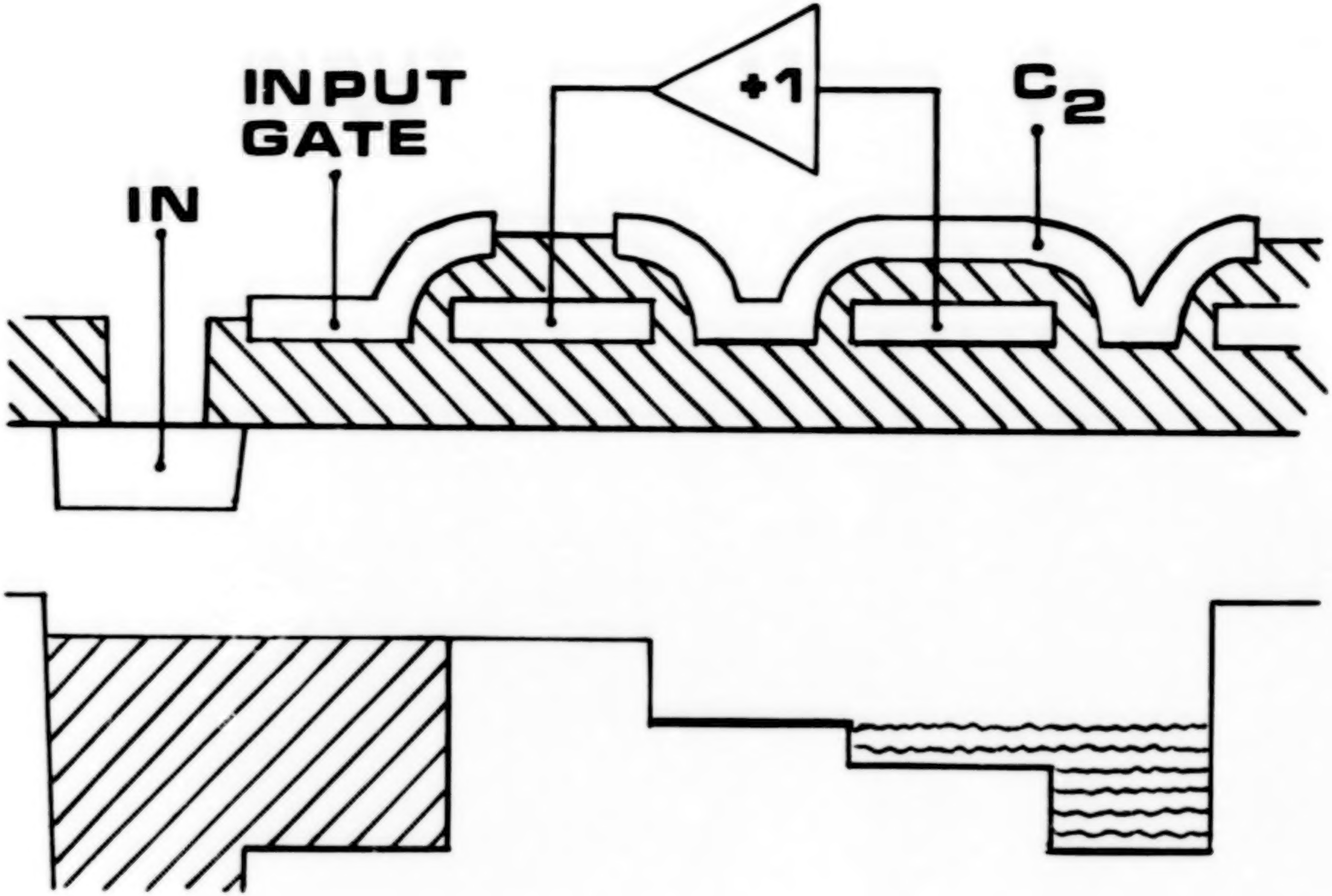

INPUT GATE
IN
+1
C_2

Figure 86.–CCD Input Stage.

TABLE OF CONTENTS

SECTION		PAGE	
I	INTRODUCTION.	1	1/A12
	A. Frequency Domain Correlation	3	1/B1
	B. Time Domain Correlation.	8	1/B6
II	32-POINT CCD CZT IC	14	1/B14
	A. Chip Overview.	14	1/B14
	B. CCD Filter	22	1/C13
	C. Operational Amplifiers	27	1/D6
	1. Design.	27	1/D6
	2. Experimental Results.	52	1/F12
	D. Multiplying Digital-to-Analog Converters (MDACs) . .	59	1/G11
	1. Design.	59	1/G11
	2. Experimental Results.	71	2/A14
	E. Read-Only Memory (ROM) and ROM Address	71	2/A14
	1. Read-Only Memory.	71	2/A14
	2. Up/Down Ring Counter (ROM Address).	82	2/C3
	3. Synchronization	87	2/C9
	F. Timing Circuitry	98	2/D10
	1. Clock Generators.	98	2/D10
	2. Experimental Results.	109	2/E10
	G. Experimental Results	114	2/F3
	H. Applications	121	2/F11
III	64-POINT CCD ANALOG/ANALOG CORRELATOR	125	2/G5
	A. Design	125	2/G5
	B. Performance Limitations in Design.	129	2/G12
	1. Multiplier Nonlinearity	129	2/G12
	2. Offsets	132	3/A4
	3. Input Stage Offsets and Nonlinearities.	133	3/A5
	C. Measured Performance	133	3/A5
	1. CCD Signal Capacity	133	3/A5
	2. Feedback Linearized Input Stage	134	3/A6

TABLE OF CONTENTS

(Continued)

SECTION PAGE

3. Multiplier Linearity. 136 3/A8
4. Offsets 140 3/A13
5. Multiplier Scale Factor Matching. 148 3/B7
6. Evaluation. 148 3/B7
D. Directions for Future Designs. 150 3/B9
1. System Organization 150 3/B9
2. CCD Design. 152 3/B11
3. Input Stage Design. 152 3/B11
4. Buffer Design 152 3/B11
5. Multipliers 153 3/B12
E. Applications and Summary 153 3/B12
1. Applications. 153 3/B12
2. Summary 153 3/B12
IV CCD BINARY/ANALOG CORRELATOR. 155 3/B14
A. Introduction 155 3/B14
B. Binary/Analog Programmable CCD Correlator Technology 159 3/C4
C. Application of Binary/Analog Correlator to Pattern Classification 171 3/D7
D. Preliminary Design of Matrix Multiplier IC 174 3/D10
E. Four-Sensor Demonstration Unit 177 3/D13
V CONCLUSIONS 182 3/E4
REFERENCES. 184 3/E6

LIST OF ILLUSTRATIONS

FIGURE PAGE

1 Block Diagram of a Transversal Filter Showing Delay Stages D and Weighting Coefficients h_n n = 0, N - 1. 2
2 Schematic of the CZT Algorithm. 5
3 Interpretation of the CZT in Terms of Chirp Input Waveforms in Chirp Filters. 6
4 Block Diagram of a CCD Programmable Correlator. 7
5 Block Diagram of the Analog/Analog Time Domain Correlator 9
6 Circuit Schematic of the Four-Quadrant Multiplier Used in the Analog/Analog Correlator of Figure 5. 10

effect is not generally modelled on SPICE simulation programs accurately, and in any case, such simulation was not available to the designer when the device was made. The only guidelines available were to attempt to keep the FET gate voltages relative to threshold fairly small, such as 3 or 4 V. Distortion from this effect was estimated at a fraction of a percent for 1 V signals.

The second major source of distortion came from the fact that the multiplier FETs did not have a voltage source on their drains, but a FET buffer with a finite output impedance. This resistance allowed the output voltage to be modulated by the loading. This problem was reduced by the feedback linearization circuitry. The buffer of the input stage was loaded with two FETs, both with their gates at the reference, or zero voltage level. The effects of this "average" load were therefore eliminated. However, the buffer output voltage could still be modulated by changes in the loading that occurred whenever a signal was presented to the gate of the multiplier FET. This would cause an attenuated gate signal to appear at the drain. Whereas the desired output current is of the form:

$$I_o = B\ V_g\ V_d$$
$$V_g = V_{gs2} - V_{gs1} \quad . \tag{17}$$

When V_d is modulated by V_g, V_d becomes

$$V_d = V_d\ (1 - B_m\ Z_b\ V_g) \quad , \tag{18}$$

and the output becomes

$$I_o = B_m V_g\ V_d\ (1 - B_m\ Z_b\ V_g)$$
$$= B_m\ (V_g\ V_d - B_m\ Z_b\ V_g^2\ V_d) \quad . \tag{19}$$

The amount of quadratic distortion is

$$D = B_m Z_b = \frac{A\ B_m}{B_b\ V_{gst(b)}} \quad , \tag{20}$$

where A is a factor that accounts for the increase in FET output impedance due to the capacitive source impedance at the gate:

$$A = (C_{source} + C_{gs})/C_{source} \quad . \tag{21}$$

The amount of distortion can be decreased by making the buffers wide (low impedance) and the multiplier FETs high impedance. The dimensions used in the design were 7.2 mils wide × 0.3 long for the buffers versus 0.5 W × 2 mils long for the resistor FETs. The B-ratio was 96, resulting in calculated distortion of about a percent at 1 V signal levels with 500 μA buffer bias current.

2. Offsets

A severe performance limitation comes from the variations in offset voltages of the 64 buffers on each CCD. This adds a random offset term to each term of each multiplication, limiting filter coefficient definition, and thus filter stopband suppression. It was estimated that the offsets would be about 30 mV rms, or about 30 dB below the 1 V signals. Assuming the offsets to be totally uncorrelated, the processing gain of 8 (square root of N) would drop the sidelobe levels to -48 dB.

However, it was not expected that the offsets would be completely uncorrelated, though a design technique was used that helped that to occur. The buffer current sources were geometrically identical to the buffers themselves, so offsets in the current sources would tend to cancel those of the buffers. Since they were within 0.4 mil of each other, reasonable correlation was expected between those two offsets. This correlation will reduce the magnitude of offsets and decrease the correlation between the offsets of adjacent buffers.

3. Input Stage Offsets and Nonlinearities

There is still a residual nonlinearity left in the transfer function of the feedback linearized input stage. Since the output equilibrates at a threshold above the input, the nonlinearities in threshold voltage versus input level would be added to the signal. These were expected to be, however, on the order of only a few tenths of a percent.

Further problems were expected from the input stage in terms of defining the absolute dc level of the output. The threshold voltage shift would have to be compensated at the input to bring the output to the desired level. This level would then have the temperature dependence of a FET threshold voltage. In this type of input stage the output voltage approaches the correct level asymptotically as 1/T. Assuming that it will never really get there, there will be a frequency dependent offset at the buffer outputs.

C. Measured Performance

1. CCD Signal Capacity

The output voltage swing available at the floating gate buffer outputs was found to be significantly smaller than the design specified. Although 2 V_{pp} had been desired, only about 0.8 V_{pp} was generally measured. Several factors were responsible for this severe problem. First, the CCD had been designed for 5 V implanted wells, but the measured change in threshold voltage was only 3.2 V. This would translate to about 2.7 V change in the CCD surface potential, or about 85% of the threshold change.

The interlevel (between first and second poly) oxide thickness was reduced between the time the device was designed and the time it was processed. This increased the parasitic loading on the floating gate and decreased the signal gain. At the calculated gain of 50%, the floating-gate output would be 1.36 V_{pp}.

The charge capacity of the phase-one well was smaller than the phase-two well that contained the floating gate, partly because the reduced interlevel oxide thickness increased the charge capacity of the phase-two well and partly because of design error. The charge capacity of the phase-one well was only about 80% of that of the well with the floating gate. That 20% reduction in output voltage swing would reduce the available voltage to 1.09 V.

Finally, with a buffer gain of 0.8, the buffer output swing would be 0.87 V_{pp}, which is in agreement with experiment.

This limitation can be overcome in a future design, since it was imposed mostly by the two-phase structure and by the inappropriate sandwiching of the floating gate under another gate, which produced much attenuation of the signal.

In general, the signal levels used were on the order of +/- 1/3 V. The measured dynamic range, limited by signal size on the top end and noise on the bottom end, was 75 dB, using external BIFET opamp output amplifiers. In a future design with 1 V signal levels at each multiplier input, the dynamic range would be increased by 20 dB.

2. Feedback Linearized Input Stage

The feedback linearized input stage performed as designed. Figure 87(a) shows a triangle wave at the CCD input with the identical triangle wave offset by a threshold at the feedback gate output. The feedback gate waveform is a sampled data signal, and the reset portion of each cycle is evident in the photo. Note that this signal is about 1.9 V_{pp}, much larger than the CCD is capable of handling. This signal is permitted at the input stage by overfilling the well. The barely visible intermediate voltage waveform in the photo shows the output voltage after charge transfer when the excess charge is left in the input stage, since all of it could not be transferred out.

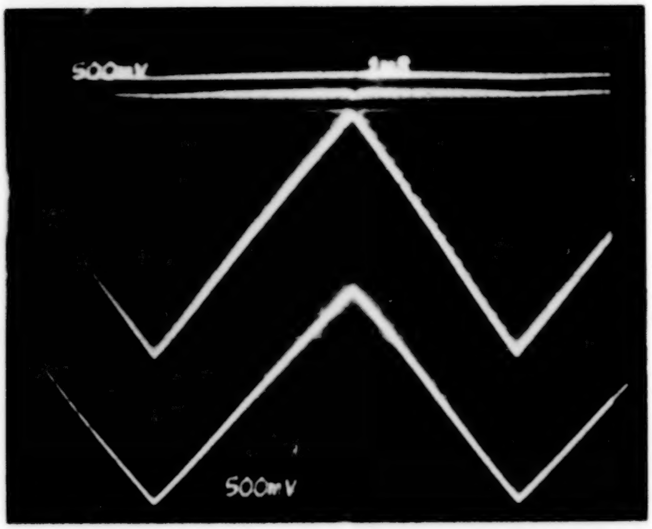


Figure 87(a).- CCD Input Stage Feedback-Linearized Output.

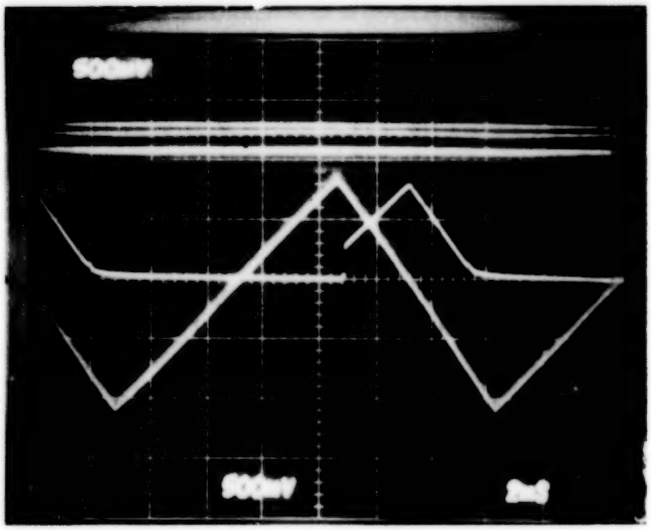


Figure 87(b).- CCD Serial Output vs Input.

Figure 87(b) shows a photograph of the CCD input feedback gate waveform, together with the waveform at the serial output buffer of the CCD. Note that the waveform is delayed by about 2.5 ms, consistent with the 25 kHz clocking frequency of the CCD, and that it saturates in the negative direction, showing the limited charge capacity of the CCD. Its output is about 0.8 V_{pp}.

The linearity of the transfer function from the CCD input diode to the serial output buffer, which should have the same waveforms as the feedback gate, was measured using a spectrum analyzer. The particular chip used had a smaller signal capacity than observed on chips from other slices. Output voltage signal swing was 0.6 V_{pp} for CCD1 (which drove the drain of the multiplier FETs) and 0.7 V_{pp} for CCD2. The spectrum analyzer outputs showed good linearity until the limits of signal swing were reached. At that point the distortion increased due to CTE loss in the case of nearly empty wells, or due to a combination of CTE loss and CCD flooding in the case of overfull or nearly full wells.

Figures 88(a) and 88(b) show CCD1 output linearity with a 4 V_{pp} and 0.5 V_{pp} signal swings, respectively. Distortion in the two cases was 0.2% and 0.28%. Figures 89(a) and 89(b) show CCD2 output linearity with 0.4 V_{pp} and 0.55 V_{pp} signal swings. Distortion in the two cases was 0.27% and 1.5%.

It is believed that performance of the input stage circuit was good, but signal swings were small enough to prohibit truly demanding tests. It is also believed that the circuit had enough problems in terms of defining dc levels, frequency dependent offsets, and the possibility of instability in some applications that its duplication in other circuits is not recommended. Other similar circuits will be discussed later.

3. Multiplier Linearity

The multipliers were tested using the circuit of Figure 90. The CCDs were disabled, and the buffer FETs were driven through the floating gate reset

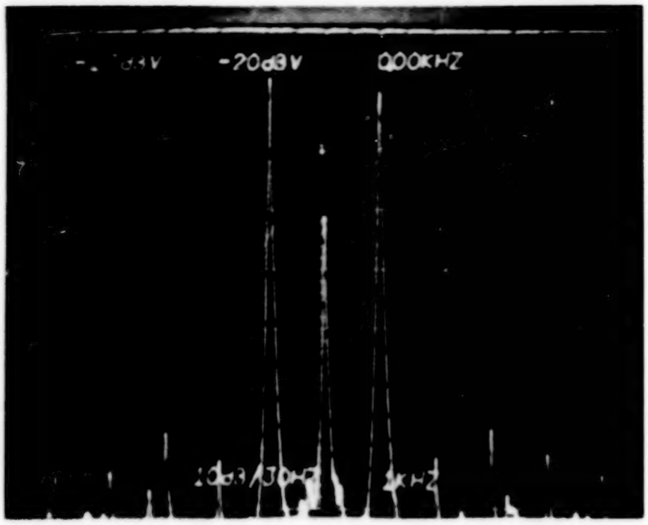


Figure 88(a).- CCD1 Serial Output Linearity 0.4 V_{pp} Signal.

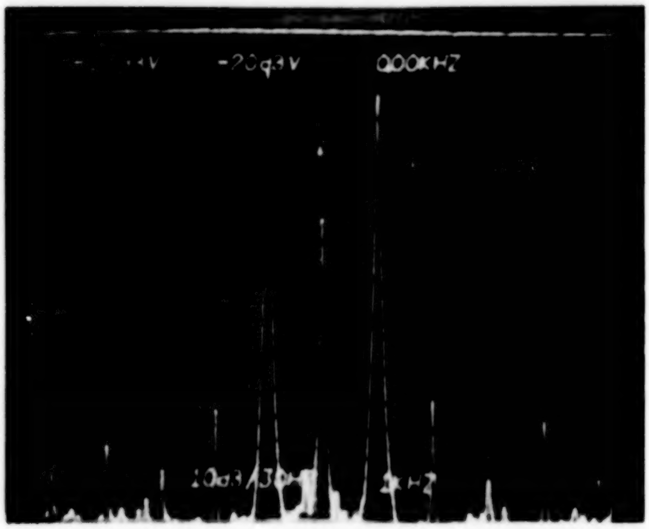


Figure 88(b).- CCD1 Serial Output Linearity 0.5 V_{pp} Signal.

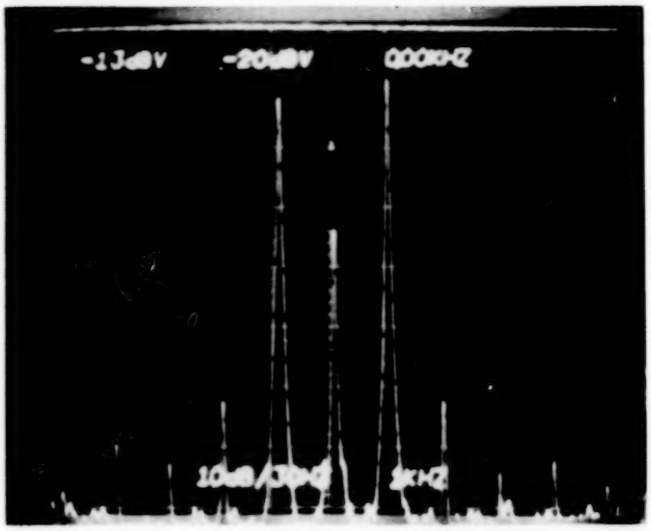


Figure 89(a).- CCD2 Serial Output Linearity 0.4 V_{pp} Signal.

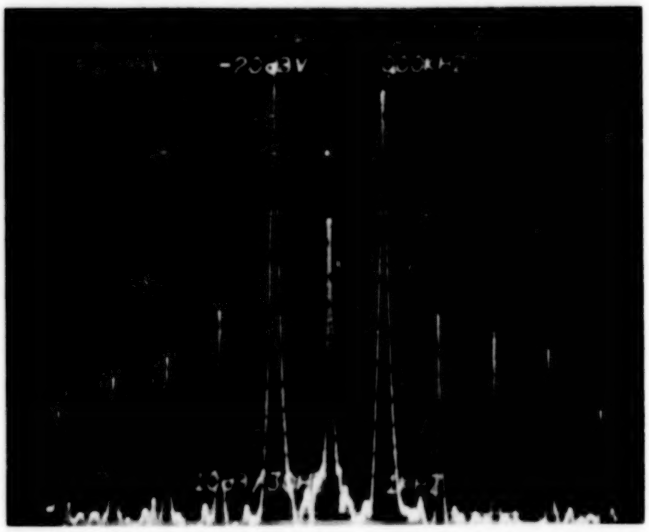


Figure 89(b).- CCD2 Serial Output Linearity 0.55 V_{pp} Signal.

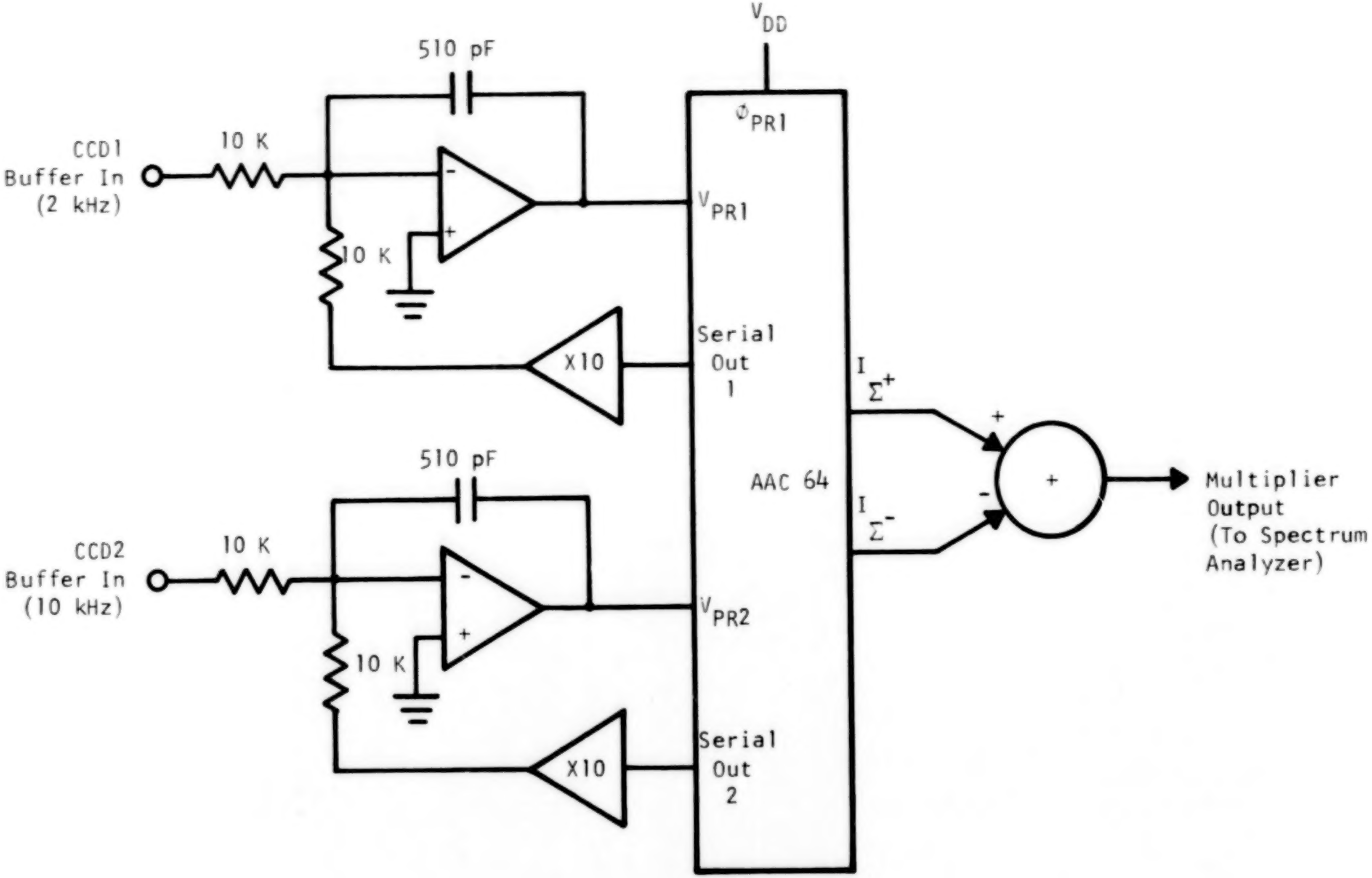

V_DD
510 pF
CCD1
Buffer In
(2 kHz)
10 K
10 K
X10
φ_PR1
V_PR1
Serial
Out
1
AAC 64
I_Σ+
I_Σ-
+
-
+
Multiplier
Output
(To Spectrum
Analyzer)
510 pF
CCD2
Buffer In
(10 kHz)
10 K
10 K
X10
V_PR2
Serial
Out
2

Figure 90.-Multiplier Linearity Test Circuit.

FETs from the floating gate reference. This circuit was placed inside the feedback loop of an opamp, which sampled the serial output of the CCD, to accomplish the feedback linearized transfer function. All multipliers were tested in parallel. Note that this arrangement allowed the multiplier to be tested with larger signals than the CCD would deliver to this circuit.

The multipliers were tested using a spectrum analyzer. The signal on the CCD1 buffers (at the multiplier FET drains) was at 2 kHz, while the CCD2 buffers were given a 10 kHz sine wave. Figures 91(a) and 91(b) show the spectral output with 0.6 V_{pp} and 2 V_{pp} sine wave inputs on both terminals. In each case, 2 kHz and 10 kHz feedthroughs due to offsets can be seen. The largest distortion terms are at 18 and 22 kHz from the buffer output impedance effects. Distortion products at 6 and 14 kHz are due to a buffer distortion effect.

At 0.3 V peak the measured multiplier distortion was about 0.3%, while at 1 V peak it measured about 1%. At the 1 V signal levels the multiplier reference FET gate voltage was increased to avoid putting the multiplier FETs in the saturation region of operation with the larger signals.

4. Offsets

The performance of the unit in terms of offset amplitudes was surprisingly good. Offsets of 30 mV_{pp} across the entire chip were measured for CCD1. Initially, offsers were measured directly in the time domain. 300 mV impulses were sent through both CCDs, giving a correlation peak equal to full scale for a single multiplier. This is shown in Figure 92(a), where the correlation peak has an amplitude of 1 V out of the current differencing amplifiers. This waveform also shows the offsets both impulses measure as they shift along the chip.

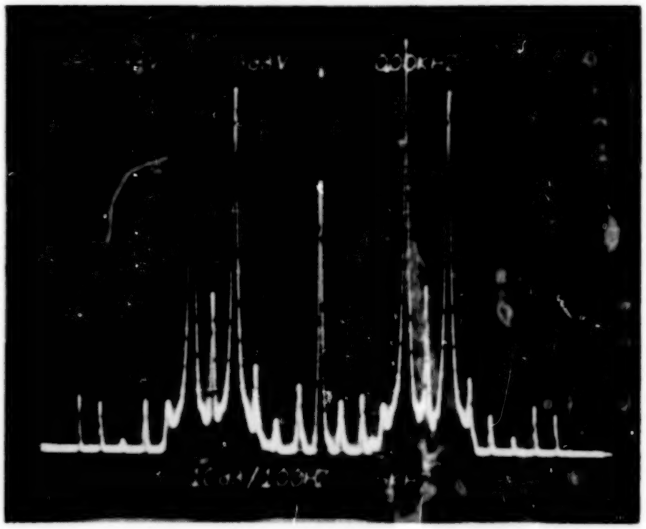


Figure 91(a).- Multiplier Output $V_{in} = \pm 0.3\ V_{pk}$.

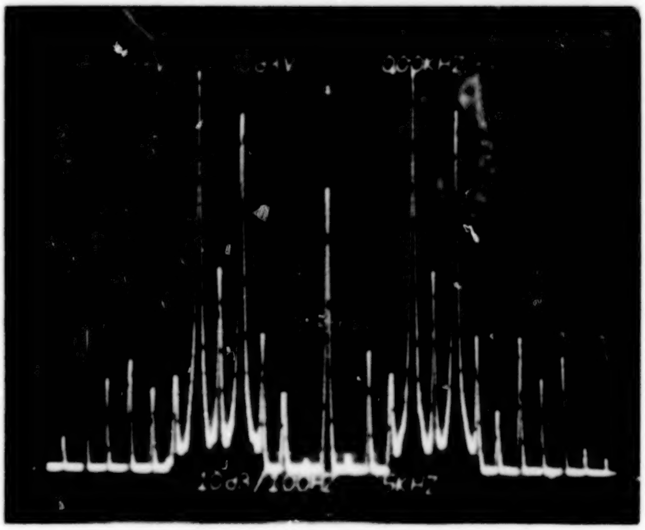
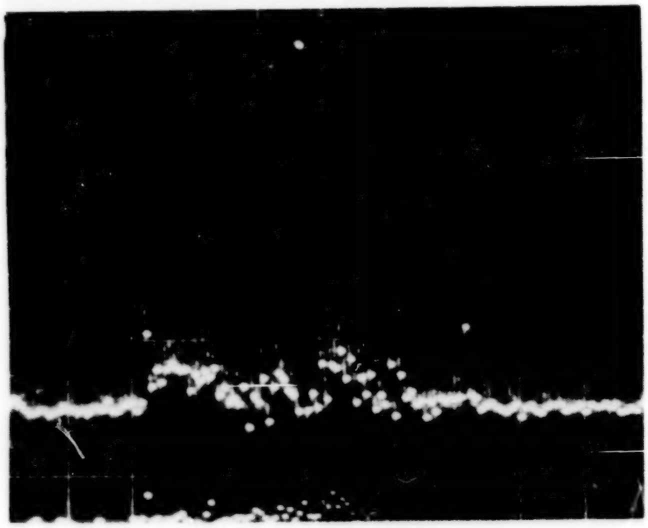
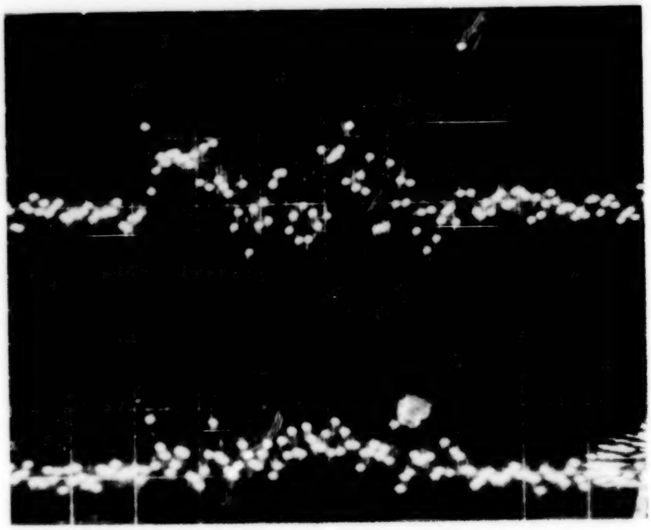


Figure 91(b).- Multiplier Output $V_{in} = \pm 1\ V_{pk}$.



200 mV/200 μs

Figure 92(a). - Convolution of Two 300 mV Impulses (CCD2 Offsets).



100 mV/200 μs

Figure 92(b). - Convolution of Impulse with CCD Offsets (CCD1 Offsets).

With impulses sent through only one of the CCDs the measured result would be an indication of the offsets of the opposite CCD tap. Figure 92(b) shows on a 2X expanded scale the results of those measurements. The top trace shows the offsets of CCD2. The offsets are within 60 mV_{pp}, except for the two endpoints, which are offset outputs from the dummy multipliers at each end of the convolver. The bottom trace shows the offsets of CCD1. They are within 30 mV_{pp}.

The offset performance of CCD1 is better than that of CCD2 for two reasons. First, the CCD1 output buffers must drive the drains of the multiplier FETs and therefore have a rather large geometry. The output buffers of CCD2 must only drive FET multiplier gates and therefore were physically smaller by a factor of 4. Since offset variations would be expected to average out over area, the offsets of these smaller buffers should be twice as large as those of CCD1.

The second reason that the offsets of the CCD2 terms were larger is that included in those offset terms is any threshold difference between the two multiplier FETs. While midway in area between the two buffer types, the corresponding multiplier FET pairs were not as physically close together, which would cause threshold variations to have a smaller degree of correlation between the two.

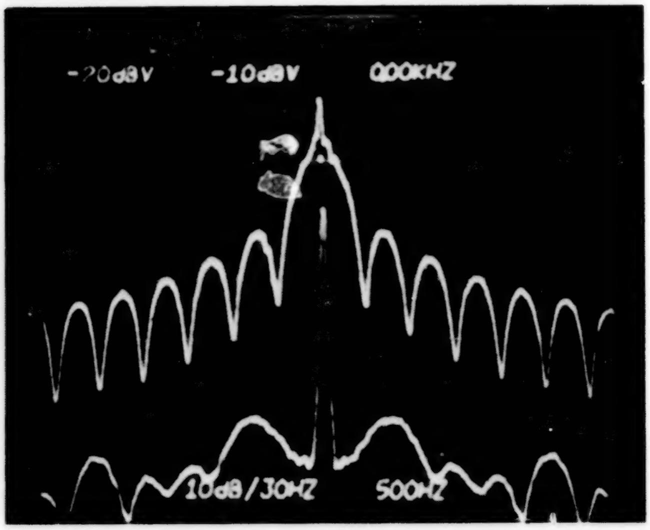
Therefore it is logical that CCD1 should have the better offset performance.

Knowing the absolute limits on the offset voltages is not enough to describe them adequately, however. Even with a knowledge of the rms value of the offsets, it is not known how they would affect the performance of a filter. For example, until it is known what the correlation is between the different offsets. If it can be assumed that the offsets are uncorrelated, then their spectrum is white, and there is a processing gain of the square root of N in summing them together.

For this reason it is advantageous to make frequency domain measurements of the offset performance. Such measurements will also give results that have a much higher signal-to-noise ratio, since the offsets of all the multipliers are being combined.

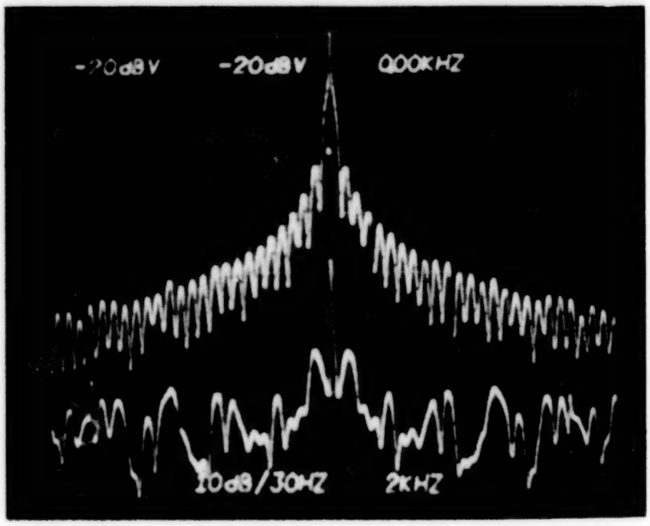
The offsets of CCD1 were measured by clocking zeroes through it, while running CCD2 from the spectrum analyzer tracking generator. Full scale can also be defined by running a large amplitude dc level through CCD1, thus implementing a square wave impulse response, or a sin(x)/x frequency response. Figure 93(a) shows the resulting outputs with full scale defined as a 0.3 V square box response in CCD1. The CCD clocking frequency is 25 kHz. The top trace shows the sin(x)/x frequency response, while the bottom trace shows the response of the offsets alone. Except below 1 kHz, the response is 50 dB below full scale. The increased amplitude at low frequencies is due to very slow variations in offset across the length of the chip. Figure 93(b) shows the same response out to 10 kHz, and Figure 94(a) shows the same result out to 25 kHz. The offset output is at a level of -50 dB out to the Nyquist frequency. Note that in Figure 94(a), there are strong offset components at the Nyquist frequency. This is due to the buffers being a mirror-image design: alternate buffers are mirror images of each other, so that the two power supply buses can be shared. This mirror-image design should therefore be avoided in future implementations.

Figure 94(b) shows the same measurements applied to determining the offset performance of CCD2. Offsets are about 10 dB worse than for CCD1. Figures 95(a) and 95(b) show CCD2 output for full scale and offset output, respectively, out to the sampling frequency.



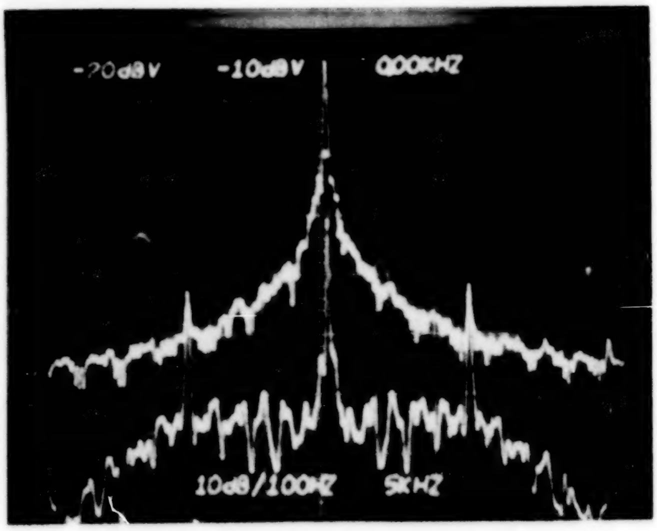
-0 dB

Figure 93(a).-CCD1 Frequency Domain Offset Measurements (Low Pass Output to 2.5 kHz).



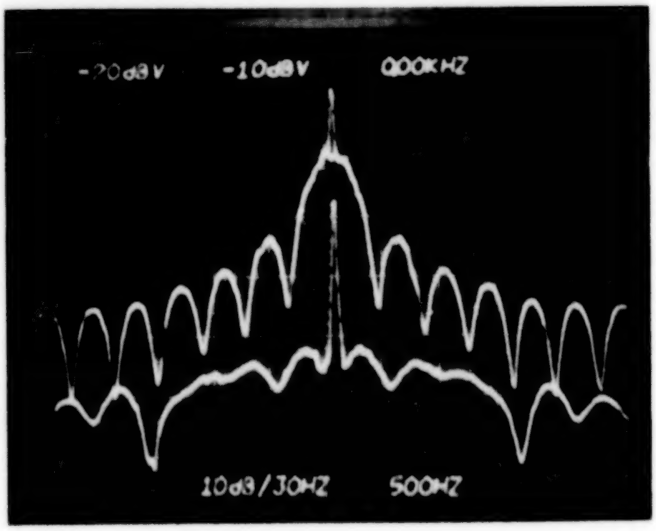
-0 dB

Figure 93(b).-CCD1 Low Pass and Offset Error Outputs to 10 kHz (Offset Error Output).



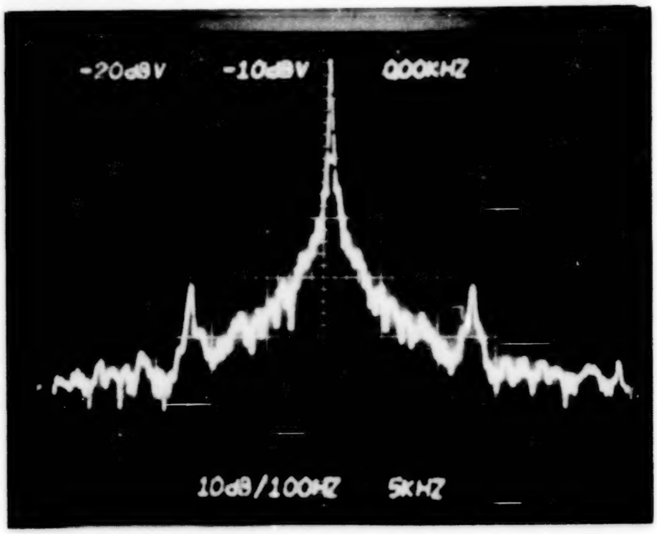
-0 dB

Figure 94(a). - CCD1 Low Pass and Offset Error Outputs to 2.5 kHz.



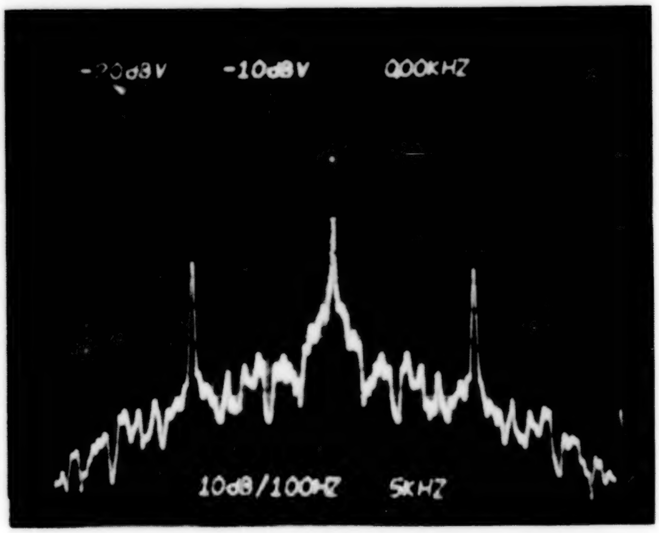
-0 dB

Figure 94(b). - CCD2 Low Pass and Offset Error Outputs to 2.5 kHz.



-0 dB

Figure 95(a). - CCD2 Low Pass Output to 25 kHz.



-0 dB

Figure 95(b). - CCD2 Offset Error Output to 25 kHz.

5. Multiplier Scale Factor Matching

Another measure of performance of the multiplier is the degree of matching of multiplier scale factors across the length of the chip. This matching was found to be within about plus or minus 1% over the entire chip. It was measured by sending an impulse through CCD1, with either plus or minus full scale in CCD2. The difference between these outputs is the multiplier scale factor. It was found that the scale factor changed very slowly, almost linearly across the chip, as if it were due to a very slow change in the oxide thickness in the multiplier FETs. Since the scale factor variations were spatially very slow, the test impulse was made four samples wide to increase the S/N ratio. Figure 96(a) shows the convolver output when the test impulse was convolved with either a plus or minus dc level. The up and down variations of the two outputs are due to offsets, while the difference in slopes is due to scale factor variations. Figure 96(b) shows the same type of measurement with the dc output levels subtracted out. The two outputs should now be superposed. The difference in slopes is seen to be very small.

6. Evaluation

There were several aspects of performance of this device that were interesting and important because they had not been tried before. The CCD feedback linearized input stage performed as expected and represents an important portion of the system. It also has the potential for use in a modified form in other CCD structures.

The CCD floating gate output performed as designed, although in the future it is recommended that alternate layouts be used that do not attenuate the CCD signal as much. This attenuation, as well as other design and processing problems, limited the signal swings to about 0.8 V_{pp}, which was the worst limitation of the device.

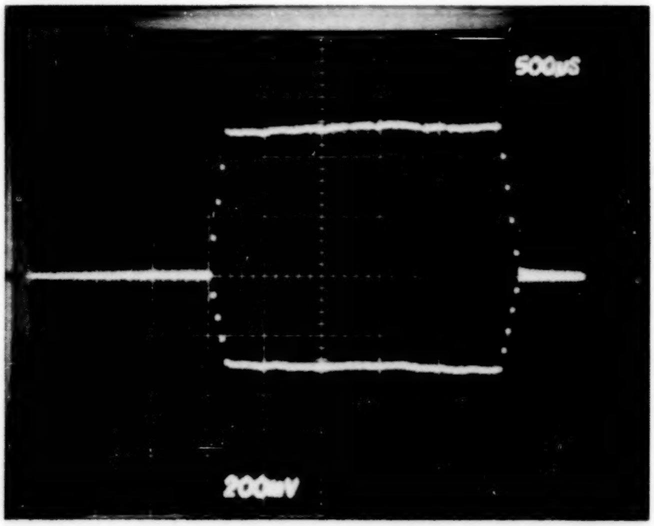


Figure 96(a).- Multiplier Scale Factor Accuracy; Convolution of CCD1 (Impulse of Four Samples) with CCD2 (Full Scale Dc).

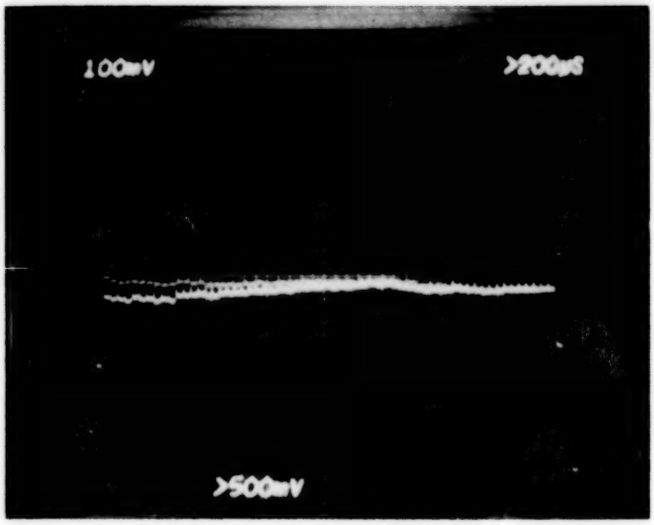


Figure 96(b).- Multiplier Scale Factor Accuracy; Multiplier Scale Factor Error.

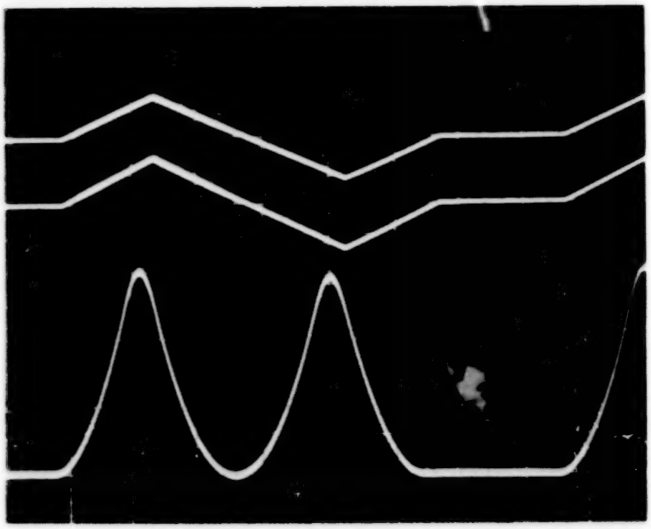
The analog multiplier performed as expected, having about 1% distortion level with 1 V signals. The buffer and multiplier offset variations were significantly better than expected, and gave perhaps the most important find from this circuit: that it is possible to achieve low offset variations in this type of correlator, with sidelobe levels typically 60 dB below 1 V signals in a 64-stage device.

Some sample outputs of the convolver in operation are shown in Figures 97(a) and 97(b). Figure 97(a) shows the convolution of two triangle waves, whose periods are very long compared to the 64 stages of convolution. The parabolic outputs are essentially the multiplication of the two triangle square waves. Again, the period of the signals is long compared to the convolution length, with the result that most of the time the output is multiplying a dc level by itself, yielding a positive result. At the square wave transitions the transitions approach the center of the convolver from opposite sides; and the result becomes the multiplication of two out-of-phase square waves, yielding a negative result.

D. Directions for Future Designs

1. System Organization

It is not felt that there are any advantages at this time to the organization wherein both signals are sent through CCDs. More preferable would be an organization where the impulse response is loaded onto an array of MOS capacitors, which would then drive the multiplier FET drain buffers. This has the advantage that a signal can be fed back after the buffer to the sample-and-hold circuitry, so that the offset term in the impulse response can be eliminated. It would also permit longer storage times of the impulse response.

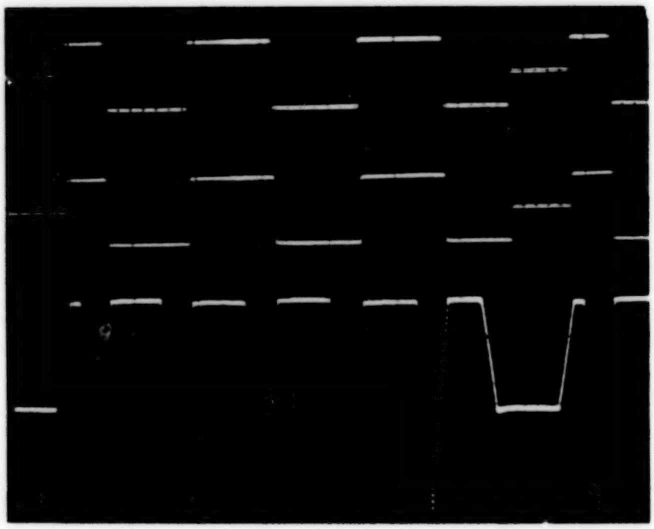


Top and Middle:
CCD1 and CCD2,
0.5 V/Div

Bottom:
Correlator Out,
2 V/Div

5 ms/Div

Figure 97(a).- 64-Point Convolution of Two Low-Frequency Triangle Waves.



Top and Middle:
CCD1 and CCD2,
Out, 0.5 V/Div

Bottom:
Correlator Out,
1 V/Div

Figure 97(b).- 64-Point Convolution of Two Low-Frequency Square Waves.

2. CCD Design

The design of the CCD will undoubtedly be quite different in future devices. The movement at TI to four-phase structures will change the ground rules for design radically. The floating gate will probably become one of the four phases, guarded on one side from moving clocks by a shield gate. The use of four-phase CCDs will result in larger signal capacity, eliminating the small signal problem of this device. In any design it will be better not to cover the floating gate with another clock electrode.

3. Input Stage Design

It is believed that the use of a linearized input stage is mandatory. The type of circuit used here performed adequately, but it would be desirable to use a circuit that had no dc level shift from the input to the output, such as a potential equilibration CCD input with feedback.

Care should be taken in the design of the input stage with respect to the loading on the output buffer. In this design a dummy stage was added with the gates of both multiplier FETs tied to the reference. This will introduce signals into the output summing bus unless the thresholds of the dummy multiplier FETs are matched exactly. They will not be matched, so the FETs should have their outputs connected to a different output ground.

4. Buffer Design

To control offsets, it is recommended that large geometry buffers be used. This is, of course, necessary in the case of the buffers that drive the drains of the multiplier FETs, but should be done also with the other buffers.

The use of mirror-image geometries from stage-to-stage in the layout of the buffers is discouraged because it generates offset components at the Nyquist frequency. The buffers and their current sources should be of matching geometries and as physically close as possible, so that their offsets will match, which will tend to make them cancel.

5. Multipliers

Several multiplier topologies are being investigated by various groups. They range from a single-transistor, time multiplexed arrangement to a four transistor bridge, which has higher linearity. Characteristics of each of these circuits are desirable, such as low offsets and high linearity, and the different possibilities should be investigated.

E. Applications and Summary

1. Applications

It is believed at this time that one of the stronger developing applications for analog/analog correlators (AAC) is adaptive filtering. It is possible that the needed circuitry for updating tap weights could be placed on the chip, resulting in a device that needed very little external support and could operate with high accuracy and dynamic range. The adaptive filtering algorithm would eliminate the effects of multiplier offset and scale factor errors and automatically update the tap weights. In this application an AAC would be much simpler to use than an analog/binary correlator, making maximum use of the strengths of the AAC (monotonicity, dynamic range), while eliminating effects from its main drawback -- offsets.

While adaptive filtering may be a strong single application, there are so many others that the analog/analog correlator should be considered a general-purpose part.

2. Summary

A 64-stage analog/analog correlator has been designed, built, and evaluated. Performance was found to be surprisingly good in spite of a major defect that reduced signal voltages by 10 dB from the design goals. The defect was in the design of the CCD floating gate outputs and limited signal swings to about 0.7 V_{pp}. Even with those limitations, dynamic range was measured at

75 dB, which means 95 dB will be achieved with the proper signal swings. When operated as a sin(x)/x lowpass filter, sidelobes due to multiplier offsets were 50 dB down from the in-band output. The -60 dB error sidelobes are therefore expected with a corrected design. Multiplier errors were found to be less than 1% at the designed signal levels and less than 0.3% at the measured smaller levels. The correlator was only operated at low speeds (100 kHz max), where speed was entirely limited by the peripheral electronics.

SECTION IV

CCD BINARY/ANALOG CORRELATOR

A. Introduction

Classification of multispectral image data is a complex data processing function for satellites that is presently performed on the ground. The goal is to perform this pattern classification in the satellite to reduce the data transmission rate required for the down link.

CCD binary/analog correlators provide a hardware implementation of the matrix multiplication function which is the kernel of the pattern classification algorithm. At present, the CCD binary/analog correlator appears to offer the optimum implementation of the matrix multiplication function. The advantages of the binary/analog correlator are given below.

- High accuracy. Since the weighting coefficients are represented in binary form, accuracy of up to 10 bits can be implemented.
- Arbitrarily long reference retention time. Since the reference is stored digitally in static shift registers, it does not need to be refreshed as the analog/analog correlator does.
- The binary/analog correlator is amenable to general-purpose IC design such that a single design can be used in a variety of system applications.

The problem is to classify vectors X

$$X = \begin{bmatrix} x_1 \\ x_2 \\ \cdot \\ \cdot \\ \cdot \\ x_N \end{bmatrix} \tag{22}$$

into classes ω_j. X is an N-element column vector, and N is the number of different wavelength sensors. The value x_k represents the amplitude of the signal in the k^{th} sensor.

A Bayes optimal pattern classifier is one which classifies patterns X into classes ω_j, j = 1, m in such a way as to maximize the discriminant

$$g_i(X) = - \sum_{j \neq i} p(X|\omega_j)\ p(\omega_j)/p(X) \quad . \tag{23}$$

In the above equation

- $p(X|\omega_j)$ is the conditional probability density function which gives the probability of occurrence of the pattern X, given that X is in fact from the class ω_j;
- $p(\omega_j)$ is the a priori probability of ω_j;
- $p(X)$ is the a priori probability of X.

Maximizing the above discriminant $g_i(X)$ is equivalent to minimizing the expected loss $L_X(i) = -g_i(X)$, which is given by

$$L_X(i) = \sum_{j \neq i} p(\omega_j|X) \quad . \tag{24}$$

In other words, $L_X(i)$ is the sum of the probabilities of classifying X in the incorrect class ($j \neq i$). Equation (23) is obtained by the use of Bayes' rule

$$p(X,\ \omega_j) = p(X|\omega_j)\ p(\omega_j) = p(\omega_j|\ X)\ p(X) \quad , \tag{25}$$

from which

$$p(\omega_j|X) = p(X|\omega_j)\ p(\omega_j)/p(X) \quad . \tag{26}$$

Since p(X) is not a function of i, maximizing $g_i(X)$ is equivalent to maximizing

$$g_i'(X) = - \sum_{j \neq i} p(X|\omega_j)\ p(\omega_j) \quad , \tag{27}$$

which, in turn, can be written as

$$g_i'(X) = p(X|\omega_i)\ p(\omega_i) - p(X) \quad . \tag{28}$$

Equation (29) is maximum if, and only if,

$$g_i'' = p(X|\omega_j)\ p(\omega_j) \tag{29}$$

is maximum. Thus, the decision rule is: $X \epsilon \omega_j$ if, and only if,

$$p(X|\omega_i)\ p(\omega_i) \geq p(X|\omega_j)\ p(\omega_j) \qquad j \neq i \quad . \tag{30}$$

This is commonly referred to as the maximum likelihood decision rule.

A quadratic classifier utilizes a Gaussian probability distribution function. In one dimension this takes the form

$$p(x|\omega_i) = (2\pi\sigma_i^{\,2})^{-\frac{1}{2}} \exp\left[-\frac{(x - \mu_i)^2}{2\sigma_i^{\,2}}\right] \quad . \tag{31}$$

Following Equation (29), it is desirable to maximize the discriminant

$$g_i''(x) = \frac{p(\omega_i)}{\sqrt{2\pi}\ \sigma_i} \exp\left[-\frac{(x - \mu_i)^2}{2\sigma_i^{\,2}}\right] \quad . \tag{32}$$

Maximizing $g_i''(x)$ is equivalent to maximizing

$$g_i'''(x) = \log g_i''(x) = \log p(\omega_i) - \tfrac{1}{2} \log 2\pi$$

$$- \log \sigma_i - \frac{(x - \mu_i)^2}{2\sigma_i^{\,2}} \quad . \tag{33}$$

Since the constant term in $-\frac{1}{2}\log 2\pi$ appears in all of the $g_i'''(x)$, it can be dropped, yielding the discriminant

$$g_i''''(x) = \log p(\omega_i) - \log \sigma_i - \frac{(x - \mu_i)^2}{2\sigma_i^2} \quad . \tag{34}$$

Returning now to N-dimensional space and assuming that all classes are equally likely on an a priori basis, the discriminant reduces to

$$g_i(X) = -\frac{1}{2}\log|\Sigma_i| - \frac{1}{2}(X - U_i)^T \Sigma_i^{-1}(X - U_i) \quad , \tag{35}$$

where

$$\Sigma_i = \begin{bmatrix} \sigma_i^{11} & \sigma_i^{12} & \cdots & \sigma_i^{1N} \\ \sigma_i^{21} & \sigma_i^{22} & \cdots & \sigma_i^{2N} \\ \cdot & & & \\ \cdot & & & \\ \cdot & & & \\ \sigma_i^{N1} & \sigma_i^{N2} & \cdots & \sigma_i^{NN} \end{bmatrix} \tag{36}$$

and

$$U_i = \begin{bmatrix} \mu_i^1 \\ \mu_i^2 \\ \cdot \\ \cdot \\ \cdot \\ \mu_i^N \end{bmatrix} \tag{37}$$

The simplified discussion given above indicates the importance of matrix multiplication to the pattern classification algorithm. In particular, computation of the form $X^T CX$ forms the kernel of the pattern classification algorithm. This computation can be implemented with binary/analog correlators.

Section IV.B discusses the binary/analog correlator technology and presents results obtained with a 32-stage x 4 bit test device.

Section IV.C discusses the application of the binary/analog correlator to the computation of X^TCX.

Section IV.D discusses the preliminary design of an IC to implement a classifier having 16 sensors with 8-bit accuracy.

Section IV.E discusses the design and implementation of a 32-stage by 8-bit binary/analog correlator unit suitable to implement a classifier having $M = 8$ bits and $N = 4$ sensors using two of the existing 32-stage by 4-bit devices.

B. Binary/Analog Programmable CCD Correlator Technology

The concept of the binary/analog correlator is illustrated in Figure 98. The weighting coefficients ($h_o h_i$ . . . h_{N-1} of Figure 1) are made electronically programmable by decomposing each one into a binary representation. h_n is represented with M-bit accuracy by

$$h_n = \sum_{k=0}^{M-1} h_n^k \, 2^{-k} \quad . \tag{38}$$

For M-bit accuracy, M parallel CCD binary/analog correlators are put on a chip as shown in Figure 98. The most significant bit h_n^o of each coefficient is loaded into the static shift register (coefficient store) shown as elongated rectangles in the filter at the top of the figure. The second most significant bit h_n^1 of each coefficient is loaded into the second coefficient store, and the least significant bit h_n^{M-1} is loaded into the coefficient store shown at the bottom of the figure. The analog input signal to be filtered is applied without attenuation to the top filter (most significant bit). The input is attenuated by a factor of two at the input of the second filter (second most significant bit), and it is attenuated by a factor of 2^{M-1} at the input to the bottom filter (least significant bit). This attenuation is performed using capacitive ratio techniques similar to those employed in MOS MDAC technology.

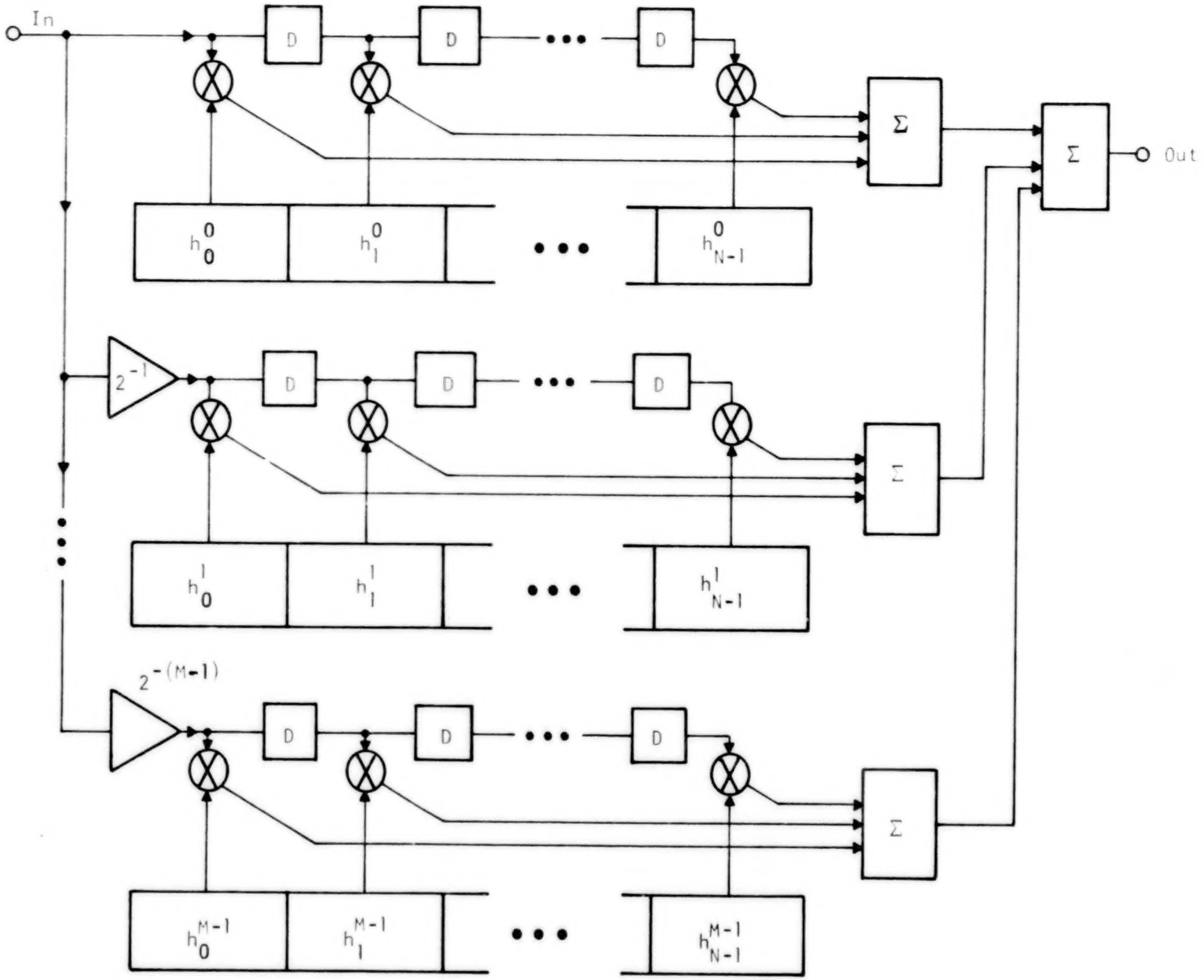

In
D
D
D
Σ
Σ
Out
h_0^0
h_1^0
h_{N-1}^0
2^{-1}
D
D
D
Σ
h_0^1
h_1^1
h_{N-1}^1
$2^{-(M-1)}$
D
D
D
Σ
h_0^{M-1}
h_1^{M-1}
h_{N-1}^{M-1}

Figure 98.-Block Diagram of the Binary/Analog Correlator.

The coefficients stored in the static shift registers then control the weighting of the transversal filters, and when the outputs of each filter are summed together as shown, the result is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \sum_{n=0}^{N=1} h_n^o Z^{-n} + 2^{-1} \sum_{n=0}^{N-1} h_n^1 z^{-n} + \ . \ . \ . + 2^{-(M-1)} \sum_{n=0}^{N-1} h_n^{M-1} z^{-n} \quad (39)$$

$$= \sum_{n=0}^{N-1} \left[\sum_{k=0}^{M-1} \left(h_n^k \, 2^{-k} \right) \right] z^{-n} \quad (40)$$

$$= \sum_{n=0}^{N-1} h_n \, z^{-n} \quad . \quad (41)$$

In the programmable CCD correlator the relative timing of charge transfer is selectively programmed. The structure is sketched in Figure 99. It consists of a conventional serial 4ϕ CCD shift register in which phase-and-a-half clocking is employed. All of the ϕ_4 electrodes are connected to a common output bus line, which is held by the output circuitry to an intermediate potential, i.e., between the OFF potential (0 V) and the ON potential (15 V). The ϕ_2 electrodes are individually clocked by a program stored in a digital shift register that is physically parallel to the CCD channel. The ϕ_1 electrodes are used as barriers at the time the charge is sensed and are clocked with a common bus line. The ϕ_2 electrodes are biased at a constant potential slightly above 0 V by a common bus line. The operation is detailed below.

Assume that at some time in the clock cycle t_1 (see Figure 99) all the signal charge packets in the CCD reside under ϕ_2 electrodes that are all in the ON state. At a later time t_2 some of the ϕ_2 electrodes are selectively turned OFF (those corresponding to program bits that are equal to 1's). Immediately after t_2, the signal charge packets will transfer from the OFF ϕ_2 electrodes through the ϕ_3 electrodes to the corresponding successive ϕ_4 electrodes which are maintained at an intermediate potential between the ON

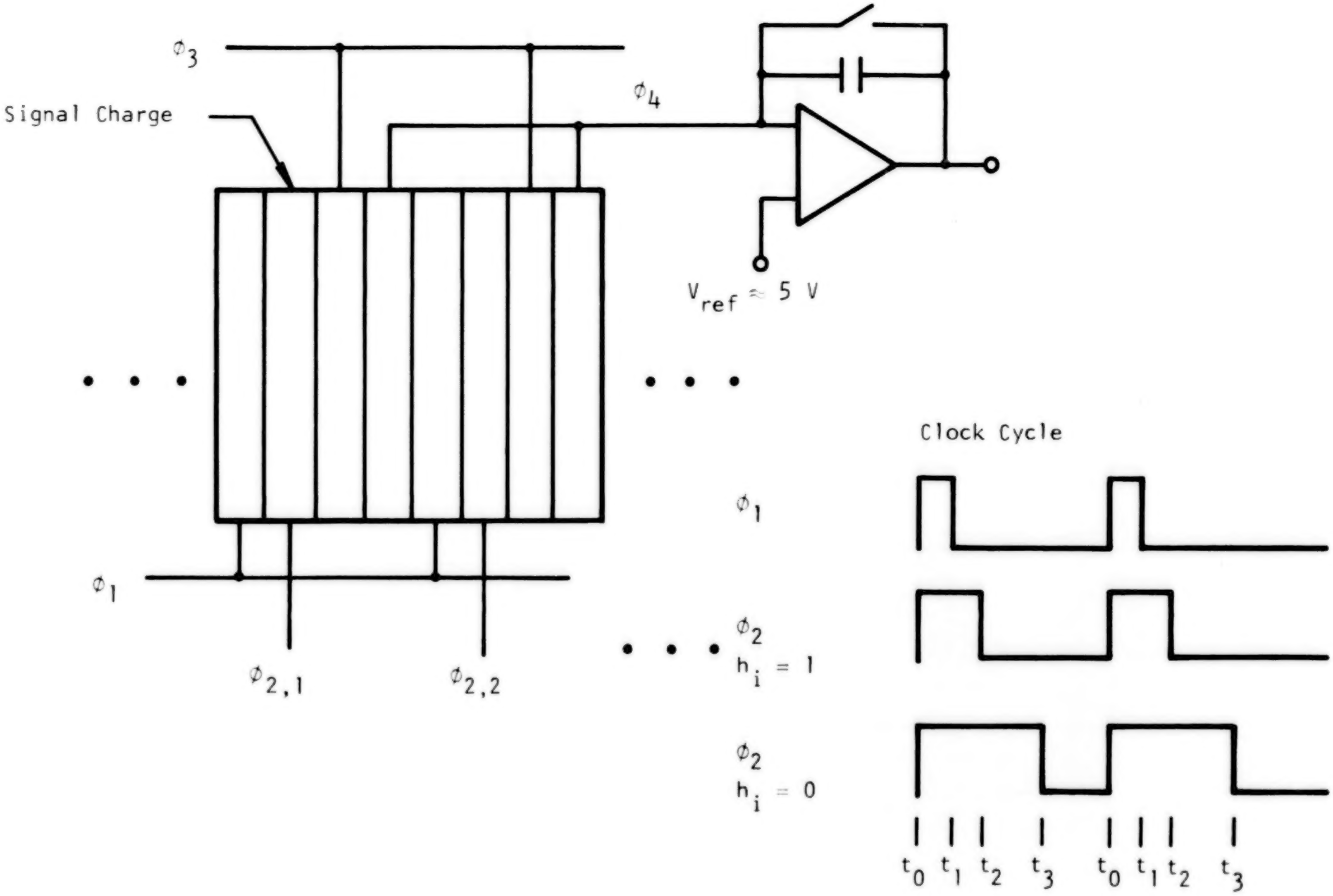

ϕ_3
ϕ_4
Signal Charge
$V_{ref} \approx 5$ V
ϕ_1
$\phi_{2,1}$
$\phi_{2,2}$
Clock Cycle
ϕ_1
ϕ_2
$h_i = 1$
ϕ_2
$h_i = 0$
t_0 t_1 t_2 t_3 t_0 t_1 t_2 t_3

Figure 99.- Schematic of the Operation of the Programmable CCD Correlator.

ϕ_1 level and the OFF ϕ_1 level. The transferred charges will be sensed and summed by the output integrator. Later in the cycle at t_3, the remaining ϕ_2 clocks are returned to ground potential and the charge packets that did not transfer at t_2 will transfer to ϕ_4 electrodes. At time t_o the ϕ_1 barrier electrodes and ϕ_2 programmed electrodes turn ON, transferring the charges from the ϕ_4 sense electrodes. At time t_o the ϕ_1 electrodes turn OFF, leaving the charges under the ϕ_2 electrodes and the cycle is repeated. The ϕ_3 electrodes serve as a buffer to prevent the transition of the ϕ_2 electrodes at time t_2 from capacitively coupling to the integrator inputs (ϕ_4). Charge is never stored under the ϕ_3 electrodes. In the time interval between t_2 and t_3 the output signal is available and is given by

$$Q_{out(n)} = \sum_{i=1}^{N} h_i \, X \, q_s(n - i). \tag{42}$$

As described thus far, the device required unipolar signals. To allow signal of either sign and to allow the CCD to operate with a fat zero charge for better charge transfer efficiency, it is desirable to operate two structures like the one just described in parallel in a differential mode. A fat zero charge Q_{fz} is inserted into each size of the differential pair, and a signal charge Q_{sig} is added to one side and substracted from the other side. The output charge will be given by

$$Q_{out(n)} = \sum_{i=1}^{N} [h_i \times (Q_{fz} + Q_{sig})] - [h_i \times (Q_{fz} - Q_{sig})] \tag{43}$$

$$Q_{out(n)} = \sum_{i=1}^{N} 2h_i \, Q_{sig} \quad . \tag{44}$$

For some applications a single-bit coefficient is adequate, but for applications requiring coefficients with multiple-bit accuracy, several differential channels may be binary weighted and combined as illustrated in Figure 100. This figure illustrates a configuration for correlating N analog samples with N digital words, each of which is represented by M bits. In this scheme the weighting is applied to the analog signals at the input of the CCD shift registers. The summing of the M parallel channels is accomplished simply by a parallel connection of the ϕ_4^+ clock buses and of the ϕ_4^- clock buses. Thus, only one output integrator is needed.

The ϕ_2 electrode clocking will be accomplished by the same shift register that stores the digital code. The circuit diagram for one stage of the shift register is shown in Figure 101. This shift register operates with three non-overlapping clocks as shown. Another signal R is used to control whether the shift register is connected serially for loading or whether each bit is continuously recirculated within the same stage in a storage mode.

The device illustrated in Figure 102 has been built to demonstrate the binary/analog concept discussed above. The device has 32 programmable taps, each having 4-bit precision. The experimental accuracy of the taps, illustrated in Figure 103, is ±1% consistent with $\frac{1}{2}$ LSB of 8-bit taps. The experimental impulse response shown in Figure 103 has a digital code -1 -7/8 -6/8 ... +7/8 in order to estimate weighting coefficient accuracy.

Figure 104 illustrates operation of the test device as a bandpass filter. Figure 104(a) is a photo of the impulse response and Figure 104(b) is of the frequency response. The center frequency is $\frac{1}{4}$ the clock frequency (f_c = 5 kHz), and the impulse response is weighted with a Hamming window quantized to 4-bit accuracy. The sidelobes in Figure 104(b) are within 1 dB of the sidelobes predicted by a computer simulation of this filter with 4-bit tap weight quantization. Figure 105 shows the frequency response of the binary/analog correlator as a bandpass filter with rectangular weighting operating at a 500 kHz

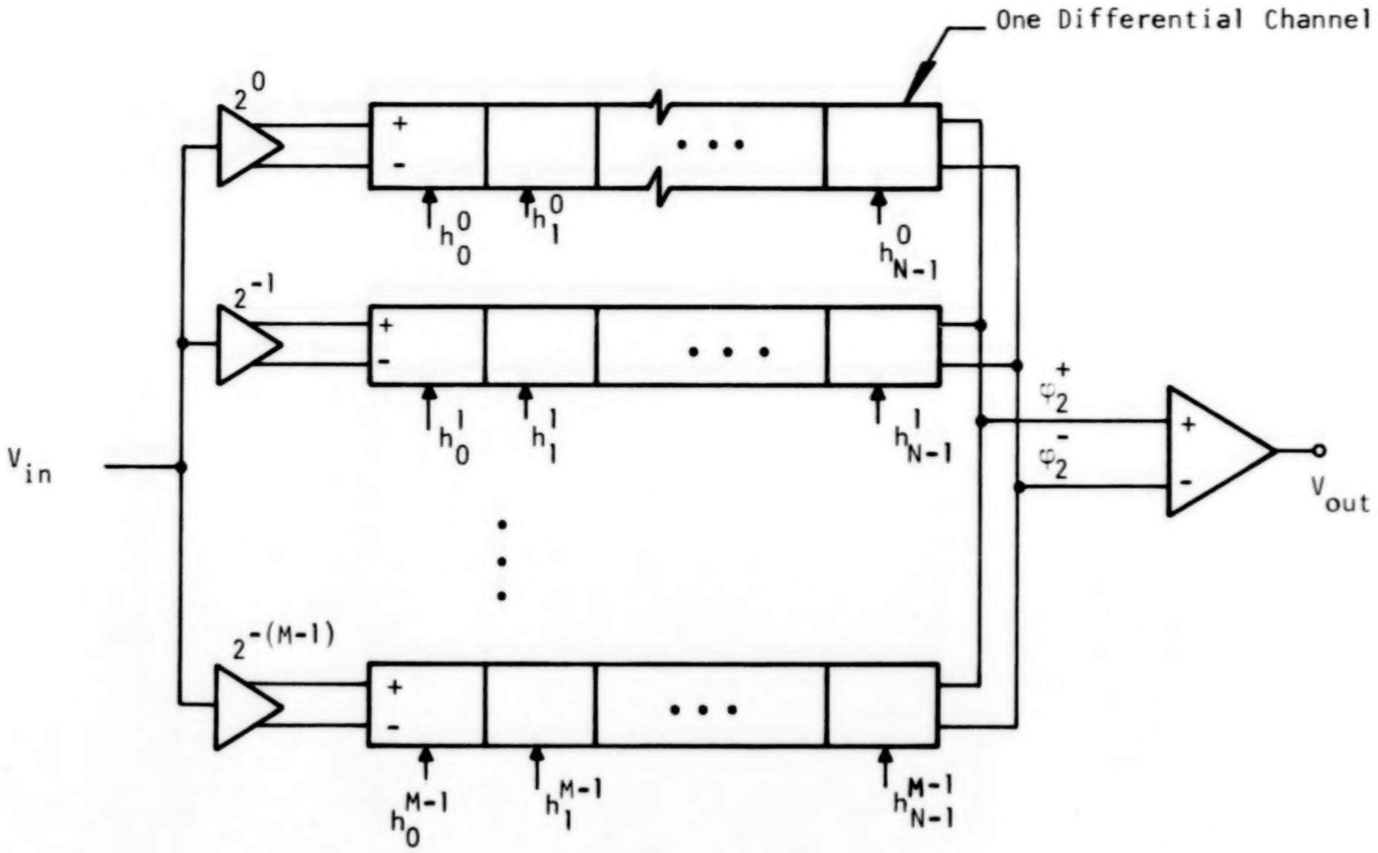

One Differential Channel
2^0
2^{-1}
$2^{-(M-1)}$
V_{in}
+
-
h_0^0
h_1^0
h_{N-1}^0
h_0^1
h_1^1
h_{N-1}^1
h_0^{M-1}
h_1^{M-1}
h_{N-1}^{M-1}
φ_2^+
φ_2^-
V_{out}

Figure 100.-Schematic of a Programmable CCD Correlator with M-bit Accuracy on the Weighting Coefficients.

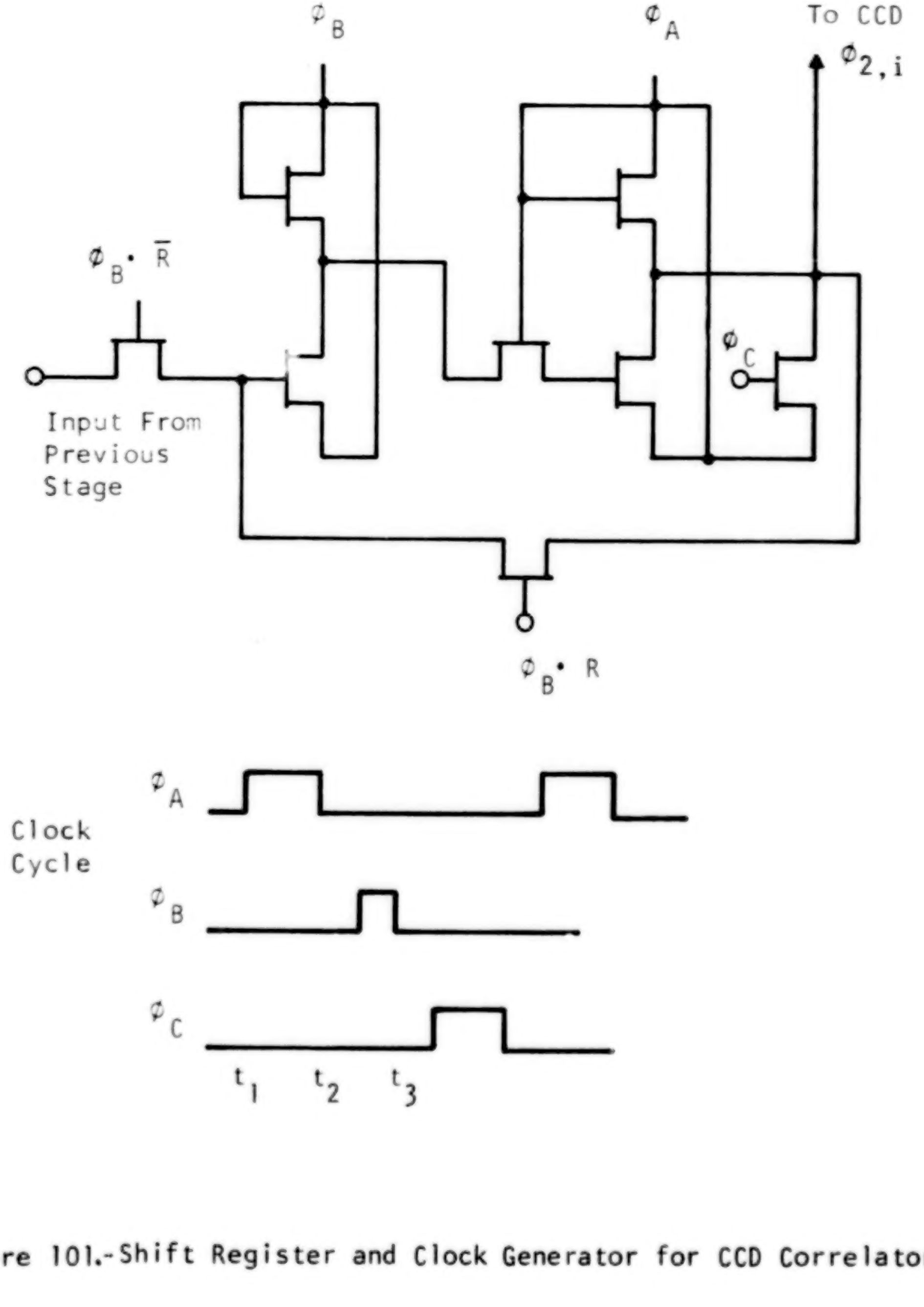

ϕB
ϕA
To CCD
ϕ2,i
ϕB · R̄
ϕC
Input From Previous Stage
ϕB · R
Clock Cycle
ϕA
ϕB
ϕC
t1
t2
t3

Figure 101.-Shift Register and Clock Generator for CCD Correlator.

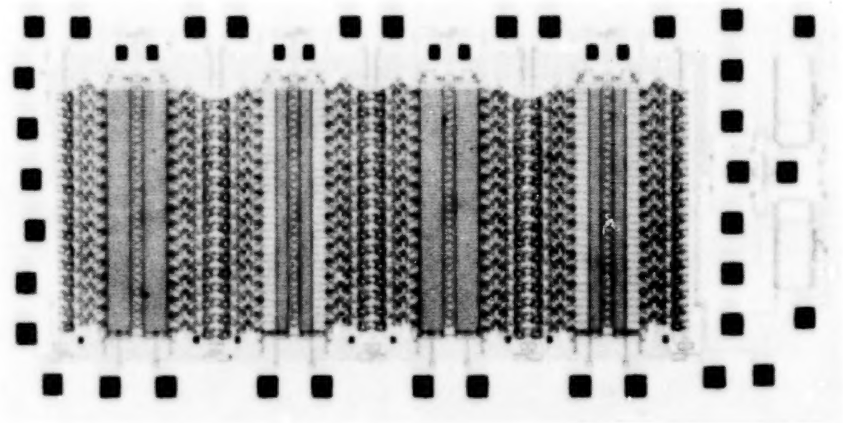
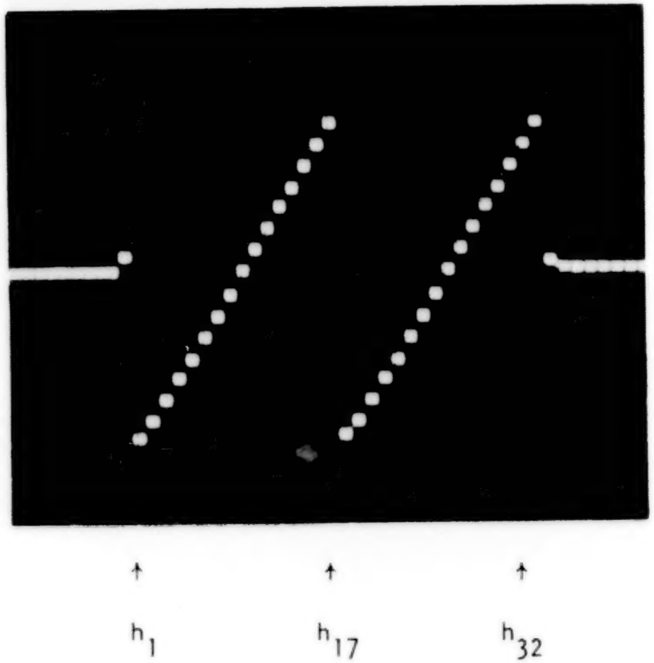


Figure 102.- Photograph of a 32-Stage Binary/Analog Correlator with Four-Bit Weighting Coefficients. This IC has eight CCD filters (two for each bit) and static shift registers to load and store 32 four-bit words. Two of these ICs can be operated in parallel to achieve eight-bit weighting coefficients. Circuitry is included on-chip to facilitate microprocessor control.

IMPULSE RESPONSE



CODE:

$h_1 = h_{17} = -1$ 1 0 0 0

$h_2 = h_{18} = -7/8$ 1 0 0 1

$h_3 = h_{19} = -6/8$ 1 0 1 0

$h_4 = h_{20} = -5/8$ 1 0 1 1

.

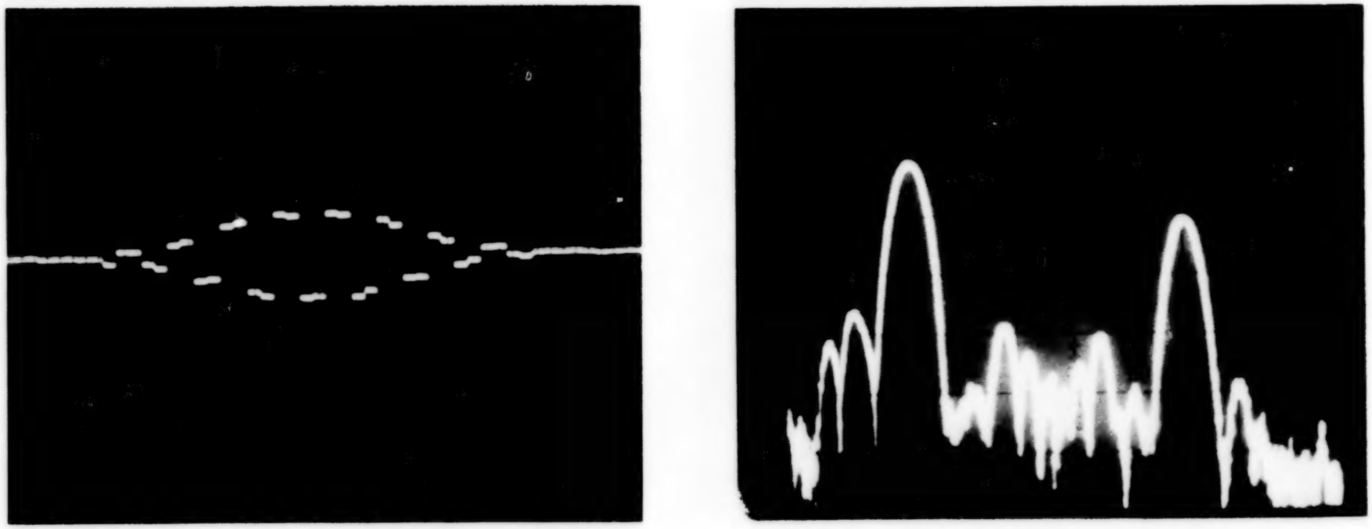
.

.

$h_{16} = h_{32} = +7/8$ 0 1 1 1

Each tap can be programmed to any arbitrary 4-bit code

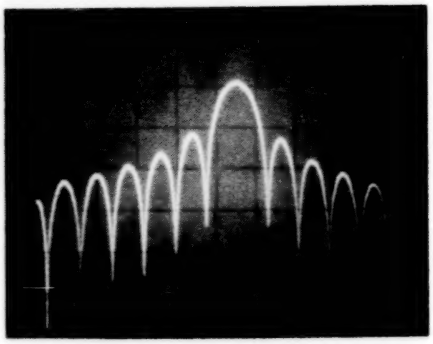
Figure 103.- Experimental Impulse Response of 32-Stage Binary/Analog Convolver.



(a) Impulse Response.

(b) Frequency Response.

Figure 104.- Response of the Test Device Operated as a Bandpass Filter.



	b_0	b_1	b_2	b_3
$h_0 = 0$	0	0	0	0
$h_1 = 7/8$	0	1	1	1
$h_2 = 0$	0	0	0	0
$h_3 = -7/8$	1	0	0	1
$h_4 = 0$	0	0	0	0

.

. etc.

.

Figure 105.- Frequency Response of the Binary/Analog Correlator Programmed to Give a Bandpass Filter with Passband at 125 kHz (Clock Frequency is 500 kHz). A rectangular window function is used. The four bits used to code the first five weighting coefficients are shown. Note 2's-complement arithmetic is used to code the negative values (h_3) with b_0 the sign bit.

clock frequency. Again, the sidelobes are within 1 dB of the computer-simulated response. The maximum clock frequency here is limited by the slew rate of the external integrating amplifier.

Figure 106 illustrates the use of the correlator for convolving p-n sequence codes. The 13-point Barker code impulse response is used. The 3 code words used for the p-n weighting are +7/8, 0, and -7/8. Shown are the correlator input, the filter impulse response, and the correlator output. The output is either 0 or +1 until the correlation peak occurs, at which time the output is +13.

C. Application of Binary/Analog Correlator to Pattern Classification

In a pattern classification system the following operation is needed:

$$X^T C X \quad , \tag{45}$$

where X is the column matrix of sensor outputs and $C = A^T A$ is a feature matrix. Let $Y = AX$ and $Y^T = X^T A^T$. To evaluate Equation (45) it is sufficient to compute

$$Y^T Y = \sum_{i=1}^{N} (y_i)^2 \quad , \tag{46}$$

where

$$y_i = \sum_{j=1}^{N} a_{ij} x_j \quad . \tag{47}$$

The computation of y_i can be accomplished using a binary/analog correlator described in Section IV.B.

Figure 107 illustrates the use of the binary/analog correlator structure in a system for the computation of $Y^T Y$. The system requires N-stages by M-bit binary/analog correlators. N correlators are required for parallel computation

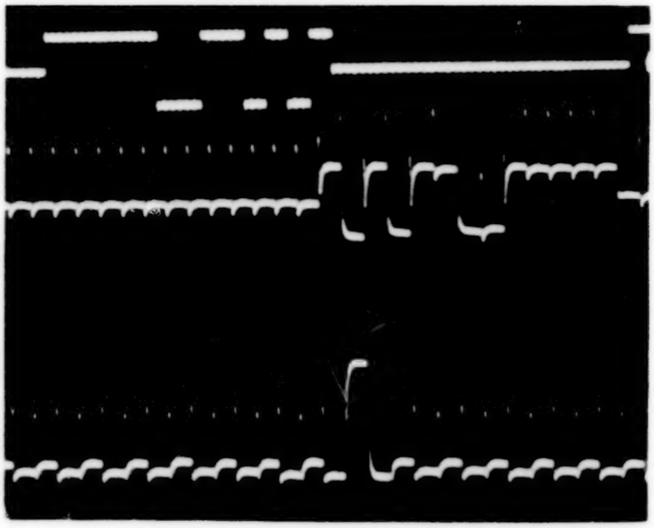


Figure 106.-Matched Filter Operation of the Test Device Using a 13-Bit Barker Code.

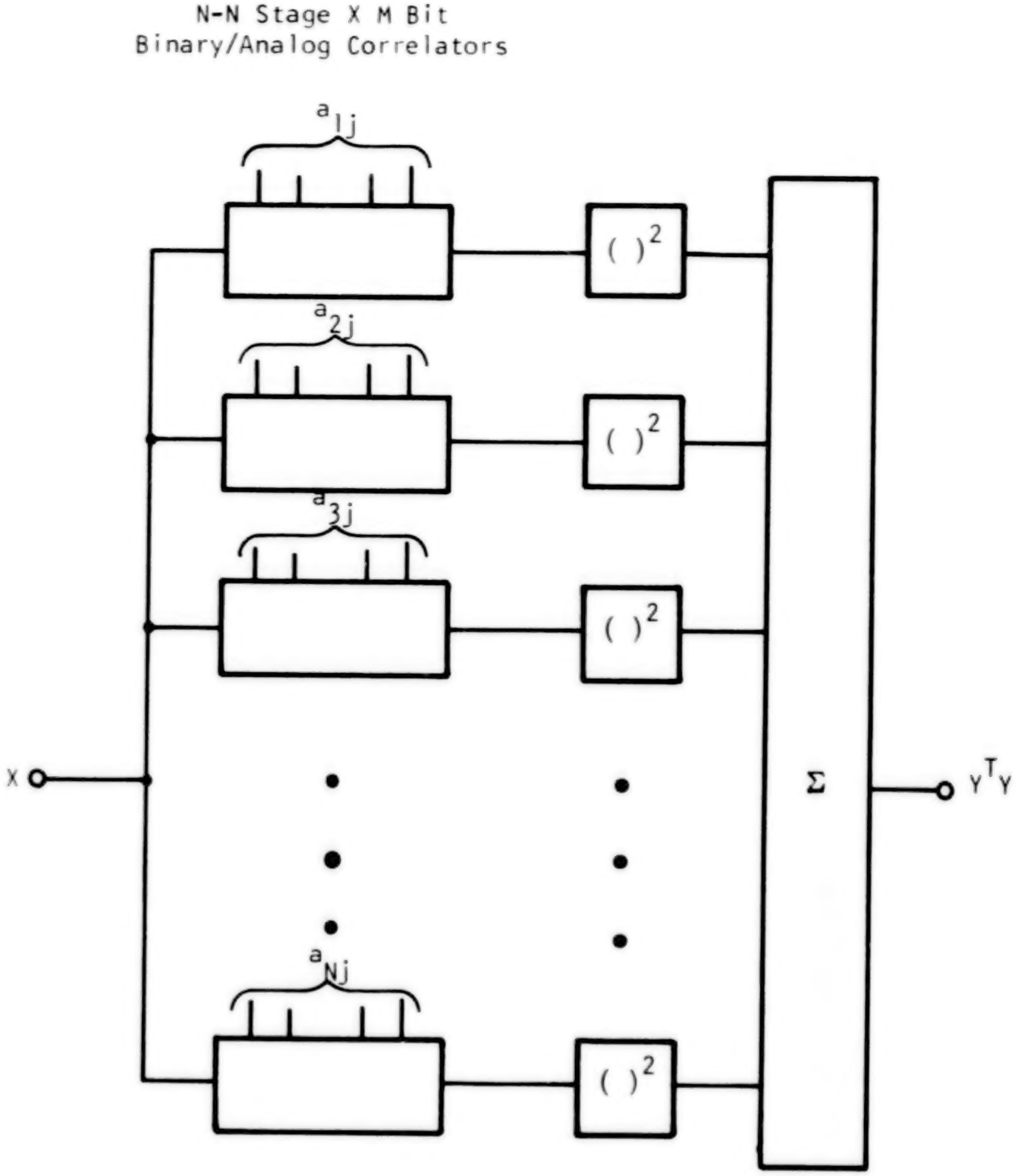

N-N Stage X M Bit
Binary/Analog Correlators
a_{1j}
a_{2j}
a_{3j}
a_{Nj}
$(\ )^2$
$(\ )^2$
$(\ )^2$
$(\ )^2$
Σ
X
Y^TY

Figure 107.- Block Diagram for Computing Y^TY.

of y_i's. The binary code stored in the i^{th} correlator is the i^{th} column of the A matrix. The output of each correlator is valid after N clock cycles, at which time X has been completely loaded into each correlator. The correlator outputs are squared and then summed together to obtain Y^TY.

D. Preliminary Design of Matrix Multiplier IC

In the desired system, the number of different colored sensors is N = 16, and M = 8 bits of accuracy are thought to be required.

In integrating the system of Figure 107 for 16 sensors, size limitations make it desirable to reduce the number of correlators on one chip to four and multiplex four chips together. The number of squaring circuits can be reduced to one by sampling the correlator outputs after N clock cycles and multiplexing these samples off chip. A block diagram of such a chip is shown in Figure 108. A preliminary layout of the IC is shown in Figure 109. This IC contains filters for four columns of the 16 x 16 feature matrix. The feature coefficients are loaded through eight reference inputs, one input for each bit of the reference. The reference inputs are TTL levels. A five bit TTL level address (four bits for row plus address enable) signal is needed to select the matrix column. An input load pulse is needed to transfer the input data to the addressed matrix column. The input signal attenuation needed for each column is realized using capacitive ratio techniques. The differential current integrator (DCI) consists of an MOS amplifier configured as an integrator. The sample-and-hold circuitry and multiplexer are realized using standard MOS techniques. All clocks are derived on-chip from the two-phase master clock. The specification on clock rate is 500 kHz (1 MHz master clock). However, the design goal will be 2 MHz (4 MHz master clock). Provisions are included for asynchronous operation wherein the data can be loaded into the correlators at high speed (greater than 2 MHz), and then the clock can be stopped to provide sufficient time ($\sim$ 2 μs) to read out the matrix product with high accuracy. Synchronizing signals for both inputs

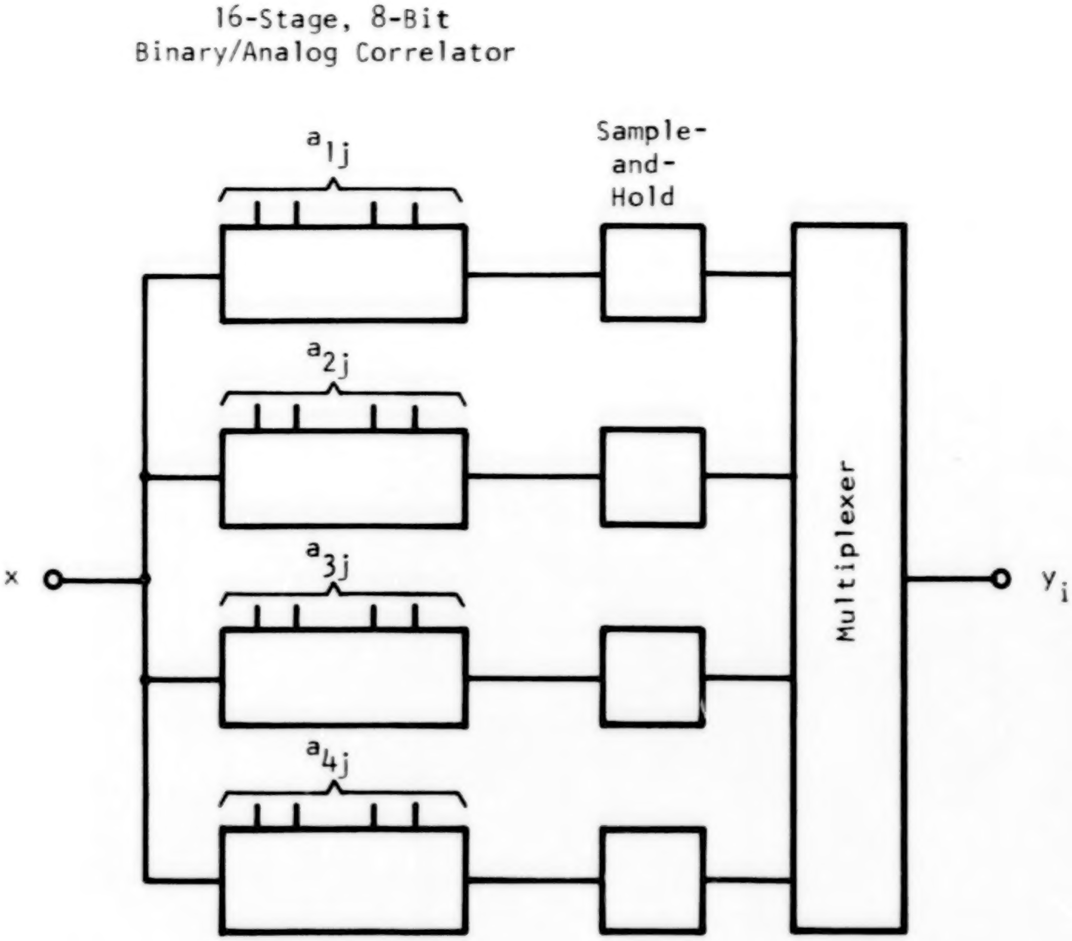
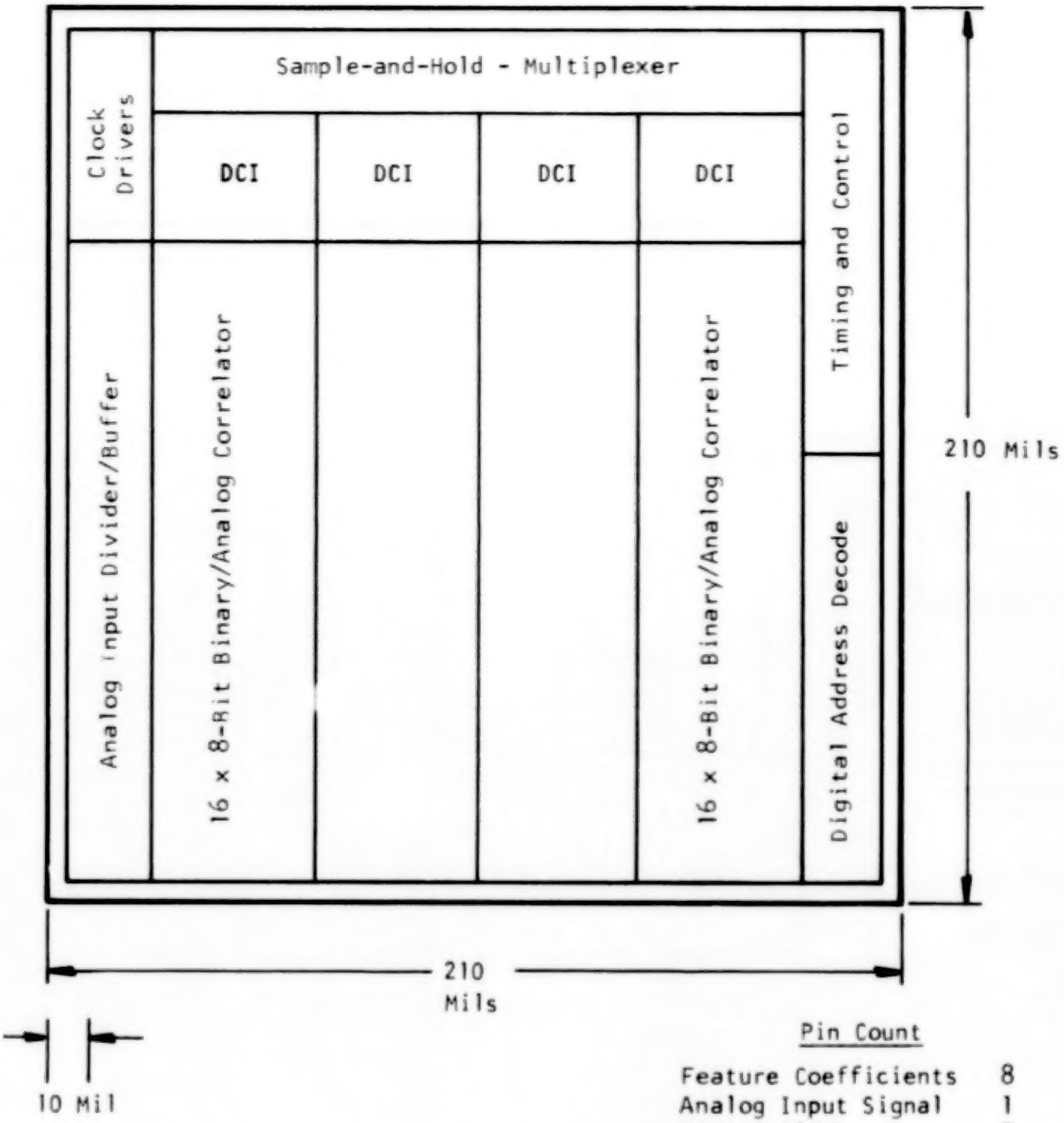

16-Stage, 8-Bit
Binary/Analog Correlator
a_{1j}
Sample-and-Hold
a_{2j}
a_{3j}
a_{4j}
x
Multiplexer
y_i

Figure 108.- Block Diagram of Binary/Analog Correlator IC.


Sample-and-Hold - Multiplexer
Clock Drivers
DCI
DCI
DCI
DCI
Timing and Control
Analog Input Divider/Buffer
16 x 8-Bit Binary/Analog Correlator
16 x 8-Bit Binary/Analog Correlator
Digital Address Decode
210 Mils
210 Mils
10 Mil

Pin Count

Feature Coefficients	8
Analog Input Signal	1
Master Clock	2
Address	5
Output	1
Sync Pulse	1
Clear Mode	1
Voltages: +12 V	1
-5 V	1
GND	1
Total	22

Figure 109.- Preliminary Design of Four-Column by 16-Stage by Eight-Bit CCD Matrix Multiplier IC.

and outputs are provided to allow interfacing to external equipment. Also, there is a provision for clearing the stored feature coefficients to zero using a digital input control signal. TTL/MOS buffers are provided for all digital inputs except the master clock. Sharp transition edges are required, and the TTL/MOS buffers required to provide these sharp edges at high speed would consume too much power to include on-chip. Dynamic range (maximum output signal/rms output noise) is expected to be 60 dB after the squaring operation.

Figure 110 illustrates the system configuration. Since this system uses parallel processing, an output is available from the accumulator every 16 clock cycles. The multiplexer is clocking the 16 correlator samples off chip to the squarer and accumulator while the correlators are being loaded with new sensor data.

The matrix multiplier system of Figure 108 must be duplicated for each feature. The pattern classification decision is then made based on the feature matrix multiplier that gives the largest result.

E. Four-Sensor Demonstration Unit

Using the 32-stage by 4-bit binary/analog correlator test devices described in Section IV.B, a 32-stage by 8-bit binary/analog correlator was constructed. This unit is suitable to implement a classifier having four sensors and 8-bit resolution. The unit is illustrated in Figure 111. To avoid using eight chips in this system, parallel processing is not used. All 16 coefficients of the 4 x 4 feature matrix are stored sequentially in the correlator. Two chips were required for eight-bit resolution. The system is operated by clocking sequences of 32 pulses through the CCDs consisting of the four-term sensor vector and 28 "zeros." The accumulator samples every fourth clock cycle. The correlator output sequence is $y_1y_2y_3y_4$ for feature 1 and $y_1y_2y_3y_4$ for feature 2. A squarer and accumulator are required to sum y_i^2 for $i = 1$ to 4 for each feature. The output will be available once every 16 clock cycles.

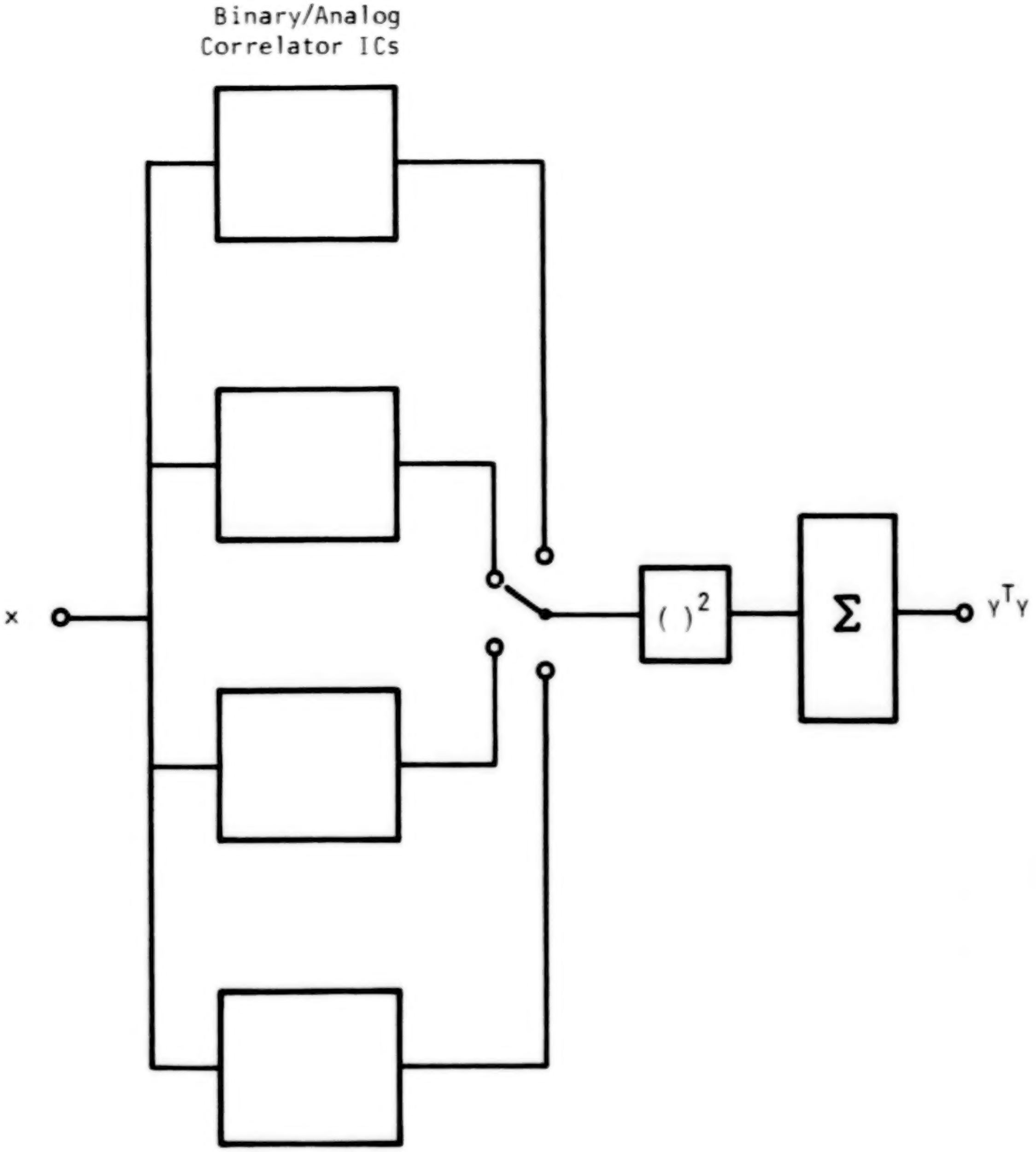

Binary/Analog
Correlator ICs
x
( )^2
Σ
$Y^T Y$

Figure 110.-System Block Diagram for Pattern Classifier.

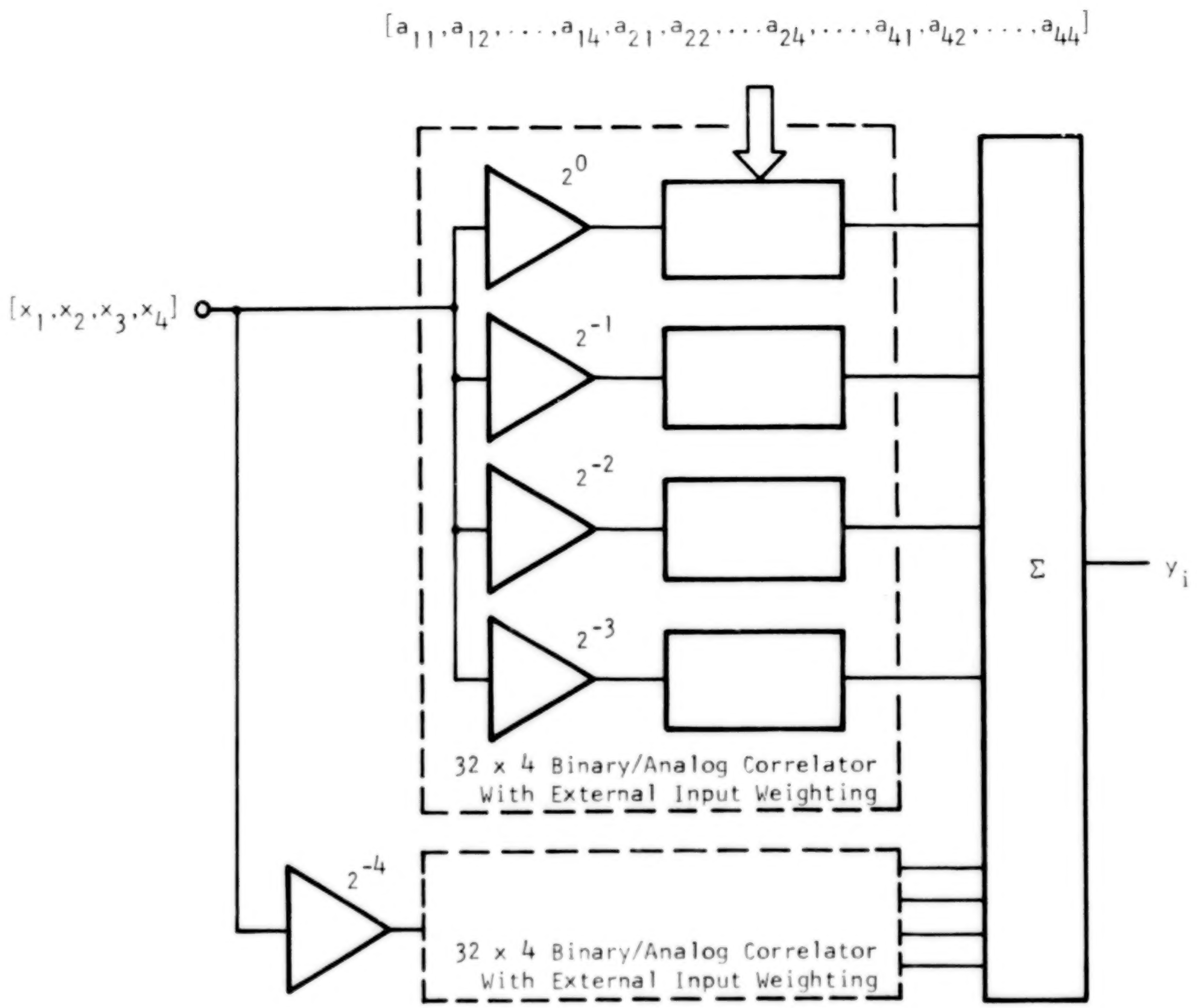
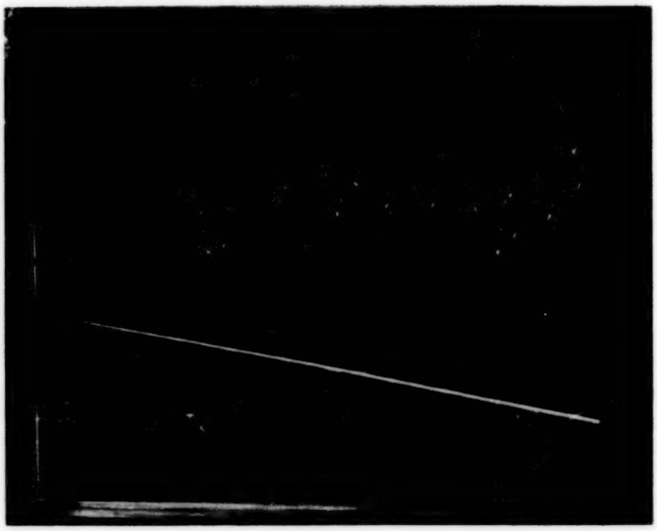

$[a_{11}, a_{12}, \ldots, a_{14}, a_{21}, a_{22}, \ldots a_{24}, \ldots, a_{41}, a_{42}, \ldots, a_{44}]$
$[x_1, x_2, x_3, x_4]$
2^0
2^{-1}
2^{-2}
2^{-3}
2^{-4}
32 x 4 Binary/Analog Correlator With External Input Weighting
32 x 4 Binary/Analog Correlator With External Input Weighting
Σ
y_i

Figure 111.- Block Diagram of Pattern Classifier Using 32 x 2-Bit Binary/Analog Correlator.

Figure 112 illustrates operation of the correlator with eight-bit accuracy. Under microprocessor control the digital code is ramped from all +127/128's to all -1's in twos-complement form. The output of the correlator (top trace) was subtracted from a 10-bit D/A converter with the same input code. The difference (bottom trace) was ±20 mV from zero error. Since the binary/analog output has a 10 V swing, this represents an accuracy of $\pm\frac{1}{2}$ LSB at eight-bits resolution.



Binary/Analog Output
(10 V Swing)

Difference Between
0/4 Converter and
Binary/Analog Outputs (±20 mV Error)

Figure 112.- Illustration of 8-Bit Accuracy of The Binary/Analog Correlator.

SECTION V

CONCLUSIONS

The objective of this program was to develop different CCD techniques for performing programmable correlation for preprocessing environmental sensor data preparatory to its transmission to the ground. Two separate ICs were developed under this program and a third IC was evaluated.

The first IC was a CCD chirp z-transform IC capable of performing a 32-point DFT at frequencies to 1 MHz. This IC, suitable for frequency domain correlation, contained MOS MDACs, CCD transversal filters, ROM, MOS amplifiers, and all needed control circuitry.

All on-chip circuitry operated as designed with the exception of the limited dynamic range caused by a fixed pattern noise due to interactions between the digital and analog circuits. Also, the tap weights of the CCD filters were erroneously shifted one bit, affecting spectral power density analysis. Both problems can easily be corrected with a minor redesign.

The second IC developed under this program was a 64-stage CCD analog/analog correlator for performing time domain correlation. Dynamic range was measured at 75 dB and potential for 95 dB dynamic range exists. Multiplier errors were found to be less than 1% at designed signal levels and less than 0.3% at the measured smaller levels. The main drawback of the analog/analog correlator is multiplier offsets, but applications exist that eliminate these effects and take advantage of the analog/analog correlator's monotonicity and dynamic range.

During the course of this program, a prototype IC for performing time domain correlation was evaluated. This IC offers digital programmability and appears to offer the optimum implementation of the matrix multiplication function needed in the pattern classification algorithm. The prototype IC was 32 stages long by 4 bits wide and operated at 500 kHz clock rate. The output dynamic range was limited to 48 dB by input signal feedthrough, but random output noise was measured to be 70 dB below the maximum output signal. The feedthrough was caused by coupling on chip and can be eliminated in future designs to be 70 dB below the maximum output signal.

It is our strong recommendation that a binary/analog correlator unit be developed suitable to implement a classifier having 8-bit accuracy and 16 sensors. We also recommend that the applications of the CZT IC to image processing problems (two dimensional processing of imagery) be explored.

In summary, the results of Contract No. NAS1-14290 were excellent. The first fully integrated CZT IC was designed and evaluated. An analog/analog correlator was designed and evaluated and an alternate approach to time domain correlation, the binary/analog correlator, was evaluated. A great deal was learned under the contract that will enable us to implement, in hardware, a pattern classifier suitable for operation in a satellite.

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7. P. Bosshart, "An Integrated Analog Correlator Using Charge-Coupled Devices," 1976 IEEE International Solid-State Circuits Conf., Digest of Technical Papers, pp 198-199, Philadelphia, February 1976.

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16. Abstract The goal of Contract No. NAS1-14290 was to develop different charged-coupled devices (CCDs) for performing programmable correlation for preprocessing environmental sensor data preparatory to its transmission to the ground. Two separate ICs were developed under this program, and a third IC was evaluated. This final report documents the results of this contract.

The first IC was a CCD chirp z-transform IC capable of performing a 32-point DFT at frequencies to 1 MHz. This IC, suitable for frequency domain correlation, contained MOS MDACs, CCD transversal filters, ROM, MOS amplifiers, and all needed control circuitry. All on-chip circuitry operated as designed with the exception of the limited dynamic range caused by a fixed pattern noise due to interactions between the digital and analog circuits.

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